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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No. 0756-2160

First Inventor or Application Identifier: Shunpei YAMAZAKI et al.

Title: ELECTRO-OPTICAL DEVICE AND ELECTRONIC DEVICE

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original, and a duplicate for fee processing)
2. [X] Specification *Total Pages* [70]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) *Total Sheets* [23]
4. [X] Oath or Declaration *Total Pages* [6]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d))
      (for continuation/divisional with Box 17 completed)
      [Note Box 5 below]
      i [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1 63(d)(2) and 1.33(b)
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein

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6. [ ] Microfiche Computer Program *(Appendix)*
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ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3 73(b) Statement [ ] Power of Attorney
   (when there is an assignee)
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement [ ] Copies of IDS Citations
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12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
14. [ ] *Small Entity [ ] Statement filed in prior application, Statement(s) Status still proper and desired
    (PTO/SB/09-12)
15. [X] Certified Copy of Japanese Priority Document
    No. 11-158797 Filed: June 4, 1999
16. [ ] Other.

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17. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment*
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ELECTRO-OPTICAL DEVICE AND ELECTRONIC DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an electro-optical device, typically an EL (electroluminescence) display device formed by a semiconductor element (an element using a semiconductor thin film) made on a substrate, and to electronic equipment (an electronic device) having the electro-optical device as a display (also referred to as a display portion).

2. Description of the Related Art

Techniques of forming a TFT on a substrate have been widely progressing in recent years, and developments of applications to an active matrix type display device are advancing. In particular, a TFT using a polysilicon film has a higher electric field effect mobility (also referred to as mobility) than a TFT using a conventional amorous silicon film, and high speed operation is therefore possible. As a result, it becomes possible to perform pixel control, conventionally performed by a driver circuit external to the substrate, by a driver circuit formed on the same substrate as the pixel.

This type of active matrix display device has been in the spotlight because of the many advantage which can be obtained by incorporating various circuits and elements on the same substrate in this type of active matrix display device, such as reduced manufacturing cost, small size, increased yield, and higher throughput.

Switching elements are formed by a TFT for each of the pixels in the active

matrix display device, current control is performed by driver elements using the switching elements, and an EL layer (electroluminescence layer) is made to emit light. A typical pixel structure at this time is disclosed in, for example, in Fig. 1 of US Patent #5,684,365 (Japanese Patent Application Laid-open No. Hei 8-234683).

As shown in Fig. 1 of the US Patent, a drain of a switching element (T1) is connected to a gate electrode of a current control element (T2), and is also connected in parallel to a capacitor (Cs). The gate voltage of the current control element (T2) is maintained by the electric charge stored in the capacitor (Cs).

Conversely, when the switching element (T1) is non-selected, the electric charge leaks through the switching element (T1) if the capacitor (Cs) is not connected (the flow of current at this point is referred to as off current), and the voltage applied to the gate electrode of the current control element (T2) becomes unable to be maintained. This is a problem which cannot be avoided because the switching element (T1) is formed by a transistor. However, the capacitor (Cs) is formed within the pixel, and therefore this becomes a factor in reducing the effective luminescence surface area (effective image display area) of the pixel.

Further, it is necessary for a large current to flow in the current control element (T2) in order to luminesce the EL layer. In other words, the performance required of the TFT becomes entirely different in the switching element and the current control element. In this type of case, it is difficult to ensure the performance required by all of the circuits and element with only one TFT structure.

SUMMARY OF THE INVENTION

In view of the above conventional technique, an object of the present invention is to provide an electro-optical device having good operation performance and high reliability, and in particular, to provide an EL display device. Another object of the present invention is to increase the quality of electronic equipment (an electronic device) having the electro-optical device as a display by increasing the image quality of the electro-optical device.

In order to achieve the above objects, the present invention assigns TFTs having an optimal structure in view of the performance required by elements contained in each pixel of the EL display device. In other words, TFTs having different structures exist within the same pixel.

Specifically, an element which places the most importance on sufficiently lowering the value of the off current (such as a switching element) is given a TFT structure in which the importance is more on reducing the off current value rather than on high speed operation. An element which places the greatest importance on current flow (such as a current control element) is given a TFT structure in which the importance is more on current flow, and on controlling deterioration due to hot carrier injection, which becomes a conspicuous problem at the same time, rather than on reducing the value of the off current.

It becomes possible to raise the operating performance of the EL display device, and to increase its reliability, with the present invention by performing proper use of TFTs on the same substrate, as above. Note that the concepts of the present invention are not limited to a pixel portion, and that the present invention is characterized by the point of being able to optimize the TFT

structure contained in the pixel portion and in a driver circuit portion for driving the pixel portion.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

Fig. 1 is a diagram showing the cross sectional structure of the pixel portion of an EL display device;

Figs. 2A and 2B are diagrams showing the top view and the composition, respectively, of the pixel portion of an EL display device;

Figs. 3A to 3E are diagrams showing manufacturing processes of an active matrix type EL display device;

Figs. 4A to 4D are diagrams showing manufacturing processes of an active matrix type EL display device;

Figs. 5A to 5C are diagrams showing manufacturing processes of an active matrix type EL display device;

Fig. 6 is a diagram showing an external view of an EL module;

Fig. 7 is a diagram showing the circuit block structure of an EL display device;

Fig. 8 is an enlarged diagram of the pixel portion of an EL display device;

Fig. 9 is a diagram showing the element structure of a sampling circuit of an EL display device;

Fig. 10 is a diagram showing the composition of the pixel portion of an EL display device;

Fig. 11 is a diagram showing the cross sectional structure of an EL display device;

Figs. 12A and 12B are diagrams showing the top view and the composition, respectively, of the pixel portion of an EL display device;

Fig. 13 is a diagram showing the cross sectional structure of the pixel portion of an EL display device;

Fig. 14 is a diagram showing the cross sectional structure of the pixel portion of an EL display device;

Figs. 15A and 15B are diagrams showing the top view and the composition, respectively, of the pixel portion of an EL display device;

Figs. 16A to 16F are diagrams showing specific examples of electronic equipment;

Figs. 17A and 17B are diagrams showing external views of an EL module;

Figs. 18A to 18C are diagrams showing manufacturing processes of a contact structure;

Fig. 19 is a diagram showing the laminate structure of an EL layer;

Figs. 20A and 20B are diagrams showing specific examples of electronic equipment;

Figs. 21A and 21B are diagrams showing the circuit composition of the pixel portion of an EL display device;

Figs. 22A and 22B are diagrams showing the circuit composition of the pixel portion of an EL display device; and

Fig. 23 is a diagram showing the cross sectional structure of the pixel

portion of an EL display device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment mode

Figs. 1 to 2B are used in explaining the preferred embodiments of the present invention. Shown in Fig. 1 is a cross sectional diagram of a pixel of an EL display device of the present invention, in Fig. 2A is its top view, and in Fig. 2B is a circuit composition. In practice, a pixel portion (image display portion) is formed with a multiple number of this type of pixel arranged in a matrix state.

Note that the cross sectional diagram of Fig. 1 shows a cross section cut along the line A-A' in the top view shown in Fig. 2A. Common symbols are used in Fig. 1 and in Figs. 2A and 2B, and therefore the three figures may be referenced as appropriate. Furthermore, two pixels are shown in the top view of Fig. 2A, and both have the same structure.

Reference numeral 11 denotes a substrate, and reference numeral 12 denotes a base film in Fig. 1. A glass substrate, a glass ceramic substrate, a quartz substrate, a silicon substrate, a ceramic substrate, a metallic substrate, or a plastic substrate (including a plastic film) can be used as the substrate 11.

Further, the base film 12 is especially effective for cases in which a substrate containing mobile ions, or a substrate having conductivity, is used, but need not be formed for a quartz substrate. An insulating film containing silicon may be formed as the base film 12. Note that the term "insulating film containing silicon" indicates, specifically, an insulating film that contains

silicon, oxygen, and nitrogen in predetermined ratios such as a silicon oxide film, a silicon nitride film, or a silicon oxynitride film (denoted by SiO_xN_y).

Two TFTs are formed within the pixel here. Reference numeral 201 denotes a TFT functioning as a switching element (hereafter referred to as a switching TFT), and reference numeral 202 denotes a TFT functioning as a current control element for controlling the amount of current flowing to an EL element (hereafter referred to as a current control TFT), and both are formed by an n-channel TFT.

The field effect mobility of the n-channel TFT is larger than the field effect mobility of a p-channel TFT, and therefore the operation speed is fast and electric current can flow easily. Further, even with the same amount of current flow, the n-channel TFT can be made smaller. The effective surface area of the display portion therefore becomes larger when using the n-channel TFT as a current control TFT, and this is preferable.

The p-channel TFT has the advantages that hot carrier injection essentially does not become a problem, and that the off current value is low, and there are already reports of examples of using the p-channel TFT as a switching TFT and as a current control TFT. However, by using a structure in which the position of an LDD region differs, the problems of hot carrier injection and the off current value in the n-channel TFT are solved by the present invention. The present invention is characterized by the use of n-channel TFTs for all of the TFTs within all of the pixels.

Note that it is not necessary to limit the switching TFT and the current control TFT to n-channel TFTs in the present invention, and that it is possible to use p-channel TFTs for either the switching TFT, the current control TFT, or both.

The switching TFT 201 is formed having: an active layer comprising a source region 13, a drain region 14, LDD regions 15a to 15d, a high concentration impurity region 16, and channel forming regions 17a and 17b; a gate insulating film 18; gate electrodes 19a and 19b, a first interlayer insulating film 20, a source wiring 21, and a drain wiring 22.

As shown in Fig. 2A, the present invention is characterized in that the gate electrodes 19a and 19b become a double gate structure electrically connected by a gate wiring 211 which is formed by a different material (a material having a lower resistance than the gate electrodes 19a and 19b). Of course, not only a double gate structure, but a so-called multi-gate structure (a structure containing an active layer having two or more channel forming regions connected in series), such as a triple gate structure, may also be used. The multi-gate structure is extremely effective in lowering the value of the off current, and by making the switching TFT 201 of the pixel into a multi-gate structure with the present invention, a low off current value can be realized for the switching TFT.

The active layer is formed by a semiconductor film containing a crystal structure. In other words, a single crystal semiconductor film may be used, and a polycrystalline semiconductor film or a microcrystalline semiconductor film may also be used. Further, the gate insulating film 18 may be formed by an insulating film containing silicon. Additionally, a conducting film can be used for all of the gate electrodes, the source wiring, and the drain wiring.

In addition, the LDD regions 15a to 15d in the switching TFT 201 are formed so as not to overlay with the gate electrodes 19a and 19b by interposing the gate insulating film 18. This structure is extremely effective in reducing the

off current value.

Note that the formation of an offset region (a region that comprises a semiconductor layer having the same composition as the channel forming regions, and to which a gate voltage is not applied) between the channel forming regions and the LDD regions is more preferable for reducing the off current value. Further, when a multi-gate structure having two or more gate electrodes is used, the high concentration impurity region formed between the channel forming regions is effective in lowering the value of the off current.

By thus using the multi-gate structure TFT as the switching TFT 201, as above, a switching element having a sufficiently low off current value is realized by the present invention. The gate voltage of the current control element can therefore be maintained for a sufficient amount of time (for a period from one selection until the next selection) without forming a capacitor (Cs), such as the one stated in the conventional example.

Namely, it becomes possible to eliminate the capacitor which causes a reduction in the effective luminescence surface area, and it becomes possible to increase the effective luminescence surface area. This means that the image quality of the EL display device can be made brighter.

Next, the current control TFT 202 is formed having: an active layer comprising a source region 31, a drain region 32, an LDD region 33, and a channel forming region 34; a gate insulating film 18; a gate electrode 35; the first interlayer insulating film 20; a source wiring 36; and a drain wiring 37. Note that the gate electrode 35 has a single gate structure, but a multi-gate structure may also be used.

As shown in Figs. 2A and 2B, the drain of the switching TFT 201 is

electrically connected to the gate of the current control TFT 202. Specifically, the gate electrode 35 of the current control TFT 202 is electrically connected to the drain region 14 of the switching TFT 201 through the drain wiring (also referred to as a connection wiring) 22. Further, the source wiring 36 is connected to an electric current supply wiring 212.

A characteristic of the current control TFT 202 is that its channel width is larger than the channel width of the switching TFT 201. Namely, as shown in Fig. 8, when the channel length of the switching TFT is taken as L1 and its channel width as W1, and the channel length of the current control TFT is taken as L2 and its channel width as W2, a relational expression is reached in which $W2 / L2 \geqq 5 \times W1 / L1$ (preferably $W2 / L2 \leqq 10 \times W1 / L1$). Consequently, it is possible for more current to easily flow in the current control TFT than in the switching TFT.

Note that the channel length L1 of the multi-gate structure switching TFT is the sum of each of the channel lengths of the two or more channel forming regions formed. A double gate structure is formed in the case of Fig. 8, and therefore the sum of the channel lengths L1a and L1b, respectively, of the two channel-forming regions becomes the channel length L1 of the switching TFT.

The channel lengths L1 and L2, and the channel widths W1 and W2 are not specifically limited to a range of values with the present invention, but it is preferable that W1 be from 0.1 to 5 μm (typically between 1 and 3 μm), and that W2 be from 0.5 to 30 μm (typically between 2 and 10 μm). It is preferable that L1 be from 0.2 to 18 μm (typically between 2 and 15 μm), and that L2 be from 0.1 to 50 μm (typically between 1 and 20 μm) at this time.

Note that it is preferable to set the channel length L in the current control

TFT on the long side in order to prevent excessive current flow. Preferably, W2 / L2 $\geqq$ 3 (more preferably W2 / L2 $\geqq$ 5). It is also preferable that the current flow per pixel is from 0.5 to 2 μA (better between 1 and 1.5 μA).

By setting the numerical values within this range, all standards, from an EL display device having a VGA class number of pixels (640 $\times$ 480) to an EL display device having a high vision class number of pixels (1920 $\times$ 1080) can be included.

Furthermore, the length (width) of the LDD region formed in the switching TFT 201 is set from 0.5 to 3.5 μm, typically between 2.0 and 2.5 μm.

The EL display device shown in Fig. 1 is characterized in that the LDD region 33 is formed between the drain region 32 and the channel forming region 34 in the current control TFT 202. In addition, the LDD region 33 has both a region which overlaps, and a region which does not overlap the gate electrode 35 by interposing a gate insulating film 18.

The current control TFT 202 supplies a current for making the EL element 203 luminesce, and at the same time controls the amount supplied and makes gray scale display possible. It is therefore necessary that there is no deterioration when the current flows, and that steps are taken against deterioration due to hot carrier injection. Furthermore, when black is displayed, the current control TFT 202 is set in the off state, but if the off current value is high, then a clean black color display becomes impossible, and this invites problems such as a reduction in contrast. It is therefore necessary to suppress the value of the off current.

Regarding deterioration due to hot carrier injection, it is known that a structure in which the LDD region overlaps the gate electrode is extremely effective. However, if the entire LDD region is made to overlap the gate

electrode, then the value of the off current rises, and therefore the applicant of the present invention resolves both the hot carrier and off current value countermeasures at the same time by a novel structure in which an LDD region which does not overlap the gate electrode is formed in series.

The length of the LDD region which overlaps the gate electrode may be made from 0.1 to 3 μm (preferable between 0.3 and 1.5 μm) at this point. If it is too long, then the parasitic capacitance will become larger, and if it is too short, then the effect of preventing hot carrier will become weakened. Further, the length of the LDD region not overlapping the gate electrode may be set from 1.0 to 3.5 μm (preferable between 1.5 and 2.0 μm). If it is too long, then a sufficient current becomes unable to flow, and if it is too short, then the effect of reducing off current value becomes weakened.

A parasitic capacitance is formed in the above structure in the region where the gate electrode and the LDD region overlap, and therefore it is preferable that this region not be formed between the source region 31 and the channel forming region 34. The carrier (electrons in this case) flow direction is always the same for the current control TFT, and therefore it is sufficient to form the LDD region on only the drain region side.

Further, looking from the viewpoint of increasing the amount of current that is able to flow, it is effective to make the film thickness of the active layer (especially the channel forming region) of the current control TFT 202 thick (preferably from 50 to 100 nm, more preferably between 60 and 80 nm). Conversely, looking from the point of view of making the off current value smaller for the switching TFT 201, it is effective to make the film thickness of the active layer (especially the channel forming region) thin (preferably from 20

to 50 nm, more preferably between 25 and 40 nm).

Next, reference numeral 41 denotes a first passivation film, and its film thickness may be set from 10 nm to 1 μm (preferably between 200 and 500 nm). An insulating film containing silicon (in particular, preferably a silicon oxynitride film or a silicon nitride film) can be used as the passivation film material. The passivation film 41 plays the role of protecting the manufactured TFT from contaminant matter and moisture. Alkaline metals such as sodium are contained in an EL layer formed on the final TFT. In other words, the first passivation film 41 works as a protecting layer so that these alkaline metals (mobile ions) do not penetrate into the TFT. Note that alkaline metals and alkaline-earth metals are contained in the term 'alkaline metal' throughout this specification.

Further, by making the passivation film 41 possess a heat radiation effect, it is also effective in preventing thermal degradation of the EL layer. Note that light is emitted from the base 11 side in the Fig. 1 structure of the EL display device, and therefore it is necessary for the passivation film 41 to have light transmitting characteristics.

A chemical compound containing at least one element selected from the group consisting of B (boron), C (carbon), and N (nitrogen), and at least one element selected from the group consisting of Al (aluminum), Si (silicon), and P (phosphorous) can be given as a light transparent material possessing heat radiation qualities. For example, it is possible to use: an aluminum nitride compound, typically aluminum nitride (Al_xN_y); a silicon carbide compound, typically silicon carbide (Si_xC_y); a silicon nitride compound, typically silicon nitride (Si_xN_y); a boron nitride compound, typically boron nitride (B_xN_y); or a

boron phosphate compound, typically boron phosphate (B_xP_y). Further, an aluminum oxide compound, typically aluminum oxide (Al_xO_y), has superior light transparency characteristics, and has a thermal conductivity of 20 $Wm^{-1}K^{-1}$, and can be said to be a preferable material. These materials not only possess heat radiation qualities, but also are effective in preventing the penetration of substances such as moisture and alkaline metals. Note that x and y are arbitrary integers for the above transparent materials.

The above chemical compounds can also be combined with another element. For example, it is possible to use nitrated aluminum oxide, denoted by AlN_xO_y, in which nitrogen is added to aluminum oxide. This material also not only possesses heat radiation qualities, but also is effective in preventing the penetration of substances such as moisture and alkaline metals. Note that x and y are arbitrary integers for the above nitrated aluminum oxide.

Furthermore, the materials recorded in Japanese Patent Application Laid-open No. Sho 62-90260 can also be used. Namely, a chemical compound containing Si, Al, N, O, and M can also be used (note that M is a rare-earth element, preferably an element selected from the group consisting of Ce (cesium), Yb (ytterbium), Sm (samarium), Er (erbium), Y (yttrium), La (lanthanum), Gd (gadolinium), Dy (dysprosium), and Nd (neodymium)). These materials not only possess heat radiation qualities, but also are effective in preventing the penetration of substances such as moisture and alkaline metals.

Furthermore, carbon films such as a diamond thin film or amorphous carbons (especially those which have characteristics close to those of diamond; referred to as diamond-like carbon) can also be used. These have very high thermal conductivities, and are extremely effective as radiation layers. Note that if

the film thickness becomes larger, there is brown banding and the transmissivity is reduced, and therefore it is preferable to use as thin a film thickness (preferably between 5 and 100 nm) as possible.

Note that the aim of the first passivation film 41 is in protecting the TFT from contaminating matter and from moisture, and therefore it must made so as to not lose this effect. A thin film made from a material possessing the above radiation effect can be used by itself, but it is effective to laminate this thin film and a thin film having shielding properties against alkaline metals and moisture (typically a silicon nitride film (Si_xN_y) or a silicon oxynitride film (SiO_xN_y)). Note that x and y are arbitrary integers for the above silicon nitride films and silicon oxynitride films.

Reference numeral 42 denotes a color filter, and reference numeral 43 denotes a fluorescent substance (also referred to as a fluorescent pigment layer). Both are a combination of the same color, and contain red (R), green (G), or blue (B). The color filter 42 is formed in order to increase the color purity, and the fluorescent substance 43 is formed in order to perform color transformation.

Note that EL display devices are roughly divided into four types of color displays: a method of forming three types of EL elements corresponding to R, G, and B; a method of combining white color luminescing EL elements with color filters; a method of combining blue or blue-green luminescing EL elements and fluorescent matter (fluorescing color change layer, CCM); and a method of using a transparent electrode as a cathode (opposing electrode) and overlapping EL elements corresponding to R, G, and B.

The structure of Fig. 1 is an example of a case of using a combination of

blue luminescing EL elements and a fluorescent substance. A blue color emitting luminescence layer is used as the EL element 203 here, light possessing blue color region wavelength, including ultraviolet light, is formed, and the fluorescent substance 43 is activated by the light, and made to emit red, green, or blue light. The color purity of the light is increased by the color filter 42, and this is outputted.

Note that it is possible to implement the present invention without being concerned with the method of luminescence, and that all four of the above methods can be used with the present invention.

Furthermore, after forming the color filter 42 and the fluorescent substance 43, leveling is performed by a second interlayer insulating film 44. A resin film is preferable as the second interlayer insulating film 44, and one such as polyimide, polyamide, acrylic, or BCB (benzocyclobutane) may be used. An inorganic film may, of course, also be used, provided that sufficient leveling is possible.

The leveling of steps due to the TFT by the second interlayer insulating film 44 is extremely important. The EL layer formed afterward is very thin. and therefore there are cases in which poor luminescence is caused by the existence of a step. It is therefore preferable to perform leveling before forming a pixel electrode so as to be able to form the EL layer on as level a surface as possible.

Furthermore, it is effective to form an insulating film having a high thermal radiation effect (hereafter referred to as a thermal radiation layer) on the second interlayer insulating film 44. A film thickness of 5 nm to 1 μm (typically between 20 and 300 nm) is preferable. This type of thermal radiation

layer functions so that the heat generated by the EL element is released, so that heat is not stored in the EL element. Further, when formed by a resin film, the second interlayer insulating film 44 is weak with respect to heat, and the thermal radiation layer works so as not to impart bad influence due to the heat generated by the EL element.

It is effective to perform leveling of the TFT by the resin film in manufacturing the EL display device, as stated above, but there has not been a conventional structure which considers the deterioration of the resin film due to heat generated by the EL element. It can therefore be said that the formation of the thermal radiation layer is extremely effective in resolving this point.

Furthermore, provided that a material which is not permeable to moisture, oxygen, or alkaline metals (a material similar to that of the first passivation film 41) is used as the thermal radiation layer, then it can also function as a protecting layer in order that alkaline metals within the EL layer do not diffuse toward the TFT, at the same time as preventing deterioration of the EL element and the resin film due to heat, as above. In addition, the thermal radiation layer also functions as a protecting layer so that moisture and oxygen do not penetrate into the EL layer from the TFT.

In particular, provided that the thermal radiation effect is desired, a carbon film such as a diamond film or a diamond-like carbon film is preferable, and in order to prevent penetration of substances such as moisture, it is more preferable to use a lamination structure of a carbon film and a silicon nitride film (or a silicon oxynitride film).

A structure in which TFT side and EL element side are segregated by an

insulating film which has a high radiation effect and is capable of shielding moisture and alkaline metal, is thus effective.

Reference numeral 45 denotes a pixel electrode (EL element anode) made from a transparent conducting film. After opening a contact hole in the second interlayer insulating film 44 and in the first passivation film 41, the pixel electrode 45 is formed so as to be connected to the drain wiring 37 of the current control TFT 202.

An EL layer (an organic material is preferable) 46, a cathode 47, and a protecting electrode 48 are formed in order on the pixel electrode 45. A single layer structure or a lamination structure can be used as the EL layer 46, but there are many cases in which the lamination structure is used. Various lamination structures have been proposed, combinations of layers such as a luminescence layer, an electron transporting layer, an electron injecting layer, a hole injecting layer, and a hole transporting layer, but any structure may be used for the present invention. Doping of a fluorescent pigment into the EL layer may also be performed, of course. Note that a luminescing element formed by a pixel electrode (anode), an EL layer, and a cathode is referred to as an EL element throughout this specification.

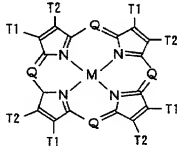
All already known EL materials can be used by the present invention. Organic materials are widely known as such materials, and considering the driver voltage, it is preferable to use an organic material. For example, the materials disclosed in the following U. S. Patents and Japanese patent applications can be used as the organic EL material:

U. S. Patent # 4, 356, 429; U. S. Patent # 4, 539, 507; U. S. Patent # 4, 720, 432; U. S. Patent # 4, 769, 292; U. S. Patent # 4, 885, 211; U. S. Patent # 4, 950, 950; U. S.

Patent # 5, 059, 861; U. S. Patent # 5, 047, 687; U. S. Patent # 5, 073, 446; U. S. Patent # 5, 059, 862; U. S. Patent # 5, 061, 617; U. S. Patent # 5, 151, 629; U. S. Patent # 5, 294, 869; U. S. Patent # 5, 294, 870; Japanese Patent Application Laid-open No. Hei 10-189525; Japanese Patent Application Laid-open No. Hei 8-241048; and Japanese Patent Application Laid-open No. Hei 8-78159.

Specifically, an organic material such as the one shown by the following general formula can be used as a hole injecting layer.

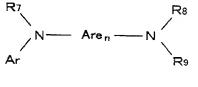
[formula 1]



Here, Q is either N or a C-R (carbon chain); M is a metal, a metal oxide, or a metal halide; R is hydrogen, an alkyl, an aralkyl, an aryl, or an alkalyl; and T1 and T2 are unsaturated six member rings including substituent such as hydrogen, alkyl, or halogen.

Furthermore, an aromatic tertiary amine can be used as an organic material hole transporting layer, preferably including the tetraaryldiamine shown by the following general formula.

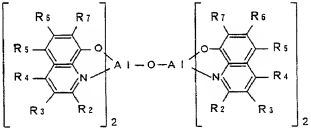
[formula 2]



In formula 2 Are is an arylene group, n is an integer from 1 to 4, and Ar, R_7, R_8, and R_9 are each various chosen aryl groups.

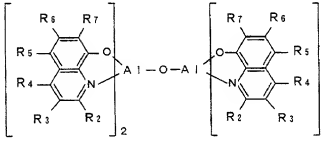
In addition, a metal oxynoid compound can be used as an organic material EL layer, electron transporting layer, or electron injecting layer. A material such as that shown by the general formula below may be used as the metal oxinoid compound.

[formula 3]



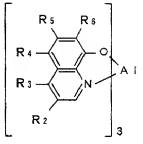
It is possible to substitute R_2 through R_7, and a metal oxinoid such as the following can also be used.

[formula 4]



In formula 4, R_2 through R_7 are defined as stated above; L_1 through L_5 are carbohydrate groups containing from 1 to 12 carbon elements; and both L_1 and L_2, or both L_2 and L_3 are formed by benzo-rings. Further, a metal oxinoid such as the following may also be used.

[formula 5]



It is possible to substitute R_2 through R_6 here. Coordination compounds having organic ligands are thus included as organic EL materials. Note that the above examples are only some examples of organic EL materials which can be used as the EL material of the present invention, and that there is absolutely no need to limit the EL material to these.

Furthermore, when using an ink jet method for forming the EL layer, it is preferable to use a polymer material as the EL material. Polymer materials such as the following can be given as typical polymer materials: polyparaphenylene vinylenes (PPVs); and polyfluorenes. For colorization, it is preferable to use, for example, a cyano-polyphenylene vinylene in a red luminescing material; a polyphenylene vinylene in a green luminescing material; and a polyphenylene vinylene and a polyalkylphenylene in a blue luminescing material. Regarding organic EL materials which can be used in an ink-jet method, all of the materials recorded in Japanese Patent Application Laid-open No. Hei 10-012377 can be cited.

Furthermore, a material containing a low work coefficient material such as magnesium (Mg), lithium (Li), cesium (Cs), barium (Ba), potassium (K), beryllium (Be), or calcium (Ca) is used as the cathode 47. Preferably, an electrode made from MgAg (a material made from Mg and Ag at a mixture of Mg:Ag = 10:1) may be used. In addition, a MgAgAl electrode, a LiAl electrode, and

a LiFAl electrode can be given as other examples. Further, the protecting electrode 48 is an electrode formed in order to be a protecting film against moisture from external to the cathode 47, and a material containing aluminum (Al) or silver (Ag) is used. The protecting electrode 48 also has a heat radiation effect.

Note that it is desirable to form the EL layer 46 and the cathode 47 in succession, without exposure to the atmosphere. In other words, no matter what type of lamination structure the EL layer and the cathode contain, it is preferable to form everything in a multi-chamber (also referred to as a cluster tool) type deposition device in succession. This is in order to avoid the absorption of moisture when the EL layer is exposed to the atmosphere because if an organic material is used as the EL layer, then it is extremely weak with respect to moisture. In addition, not only the EL layer 46 and the cathode 47, it is even better to form all the way through the protecting electrode 48 in succession.

The EL layer is extremely weak with respect to heat, and therefore it is preferable to use vacuum evaporation (in particular, an organic molecular beam evaporation method is effective in that it forms a very thin film, on the molecular order level), sputtering, plasma CVD, spin coating, screen printing, or ion plating as the film deposition method. It is also possible to form the EL layer by an ink-jet method. For the ink jet method there is a bubble jet method using cavitation (refer to Japanese Patent Application Laid-open No. Hei 5-116297), and there is a piezo method using a piezo element (refer to Japanese Patent Application Laid-open No. Hei 8-290647), and in view of the fact that organic EL materials are weak with respect to heat, the piezo method is

preferable.

Reference numeral 49 denotes a second passivation film, and its film thickness may be set from 10 nm to 1 μm (preferable between 200 and 500 nm). The object of forming the second passivation film 49 is mainly to protect the EL layer 46 from moisture, but it is also good if the second passivation film 49 is made to possess a heat radiation effect, similar to the first passivation film 41. The same materials as used for the first passivation film 41 can therefore be used as the formation material of the second passivation film 49. Note that when an organic material is used as the EL layer 46, it deteriorates due to bonding with oxygen, and therefore it is preferable to use an insulating film which does not easily emit oxygen.

Further, the EL layer is weak with respect to heat, as stated above, and therefore it is preferable to perform film deposition at a low temperature as possible (preferably in the range from room temperature to 120°C). It can therefore be said that plasma CVD, sputtering, vacuum evaporation, ion plating, and solution application (spin coating) are desirable film deposition methods.

The EL display device of the present invention has a pixel portion containing a pixel with a structure as stated above, and TFTs having differing structures in response to their function are arranged in the pixel. A switching TFT having a sufficiently low off current value, and a current control TFT which is strong with respect to hot carrier injection can be formed within the same pixel, and an EL display device having high reliability and which is capable of good image display can thus be formed.

Note that the most important point in the pixel structure of Fig. 1 is that a multi-gate structure TFT is used as the switching TFT, and that it is not

necessary to place limits on the structure of Fig. 1 with regard to such things as the placement of LDD regions.

A more detailed explanation of the present invention, having the above constitution, is now performed by the embodiments shown below.

Embodiment 1

The embodiments of the present invention are explained using Figs. 3A to 5C. A method of manufacturing a pixel portion, and TFTs of a driver circuit portion formed in the periphery of the pixel portion, is explained here. Note that in order to simplify the explanation, a CMOS circuit is shown as a basic circuit for the driver circuits.

First, as shown in Fig. 3A, a base film 301 is formed with a 300 nm thickness on a glass substrate 300. Silicon oxynitride films are laminated as the base film 301 in embodiment 1. It is good to set the nitrogen concentration to between 10 and 25 wt% in the film contacting the glass substrate 300.

Further, it is effective to form a heat radiating layer, made from the same material as that of the first passivation film 41 shown in Fig. 1, as a portion of the base film 301. A large electric current flows in a current control TFT, heat is easily generated, and therefore it is effective to form the heat radiating layer as close as possible to the current control TFT.

Next, an amorphous silicon film (not shown in the figures) is formed with a thickness of 50 nm on the base film 301 by a known deposition method. Note that it is not necessary to limit this to the amorphous silicon film, and another film may be formed provided that it is a semiconductor film containing an

amorphous structure (including a microcrystalline semiconductor film). In addition, a compound semiconductor film containing an amorphous structure, such as an amorphous silicon germanium film, may also be used. Further, the film thickness may be made from 20 to 100 nm.

The amorphous silicon film is then crystallized by a known method, forming a crystalline silicon film (also referred to as a polycrystalline silicon film or a polysilicon film) 302. Thermal crystallization using an electric furnace, laser annealing crystallization using a laser, and lamp annealing crystallization using an infrared lamp exist as known crystallization methods. Crystallization is performed in embodiment 1 using light from an excimer laser which uses XeCl gas.

Note that pulse emission type excimer laser light formed into a linear shape is used in embodiment 1, but a rectangular shape may also be used, and continuous emission argon laser light and continuous emission excimer laser light can also be used.

The crystalline silicon film is used as an active layer of the TFTs in embodiment 1, but it is also possible to use an amorphous silicon film as the active layer. However, it is necessary for a large current to flow through the current control TFT, and therefore it is more effective to use the crystalline silicon film, through which current easily flows.

Note that it is effective to form the active layer of the switching TFT, in which there is a necessity to reduce the off current, by the amorphous silicon film, and to form the active layer of the current control TFT by the crystalline silicon film. Electric current flows with difficulty in the amorphous silicon film because the carrier mobility is low, and the off current does not easily

flow. In other words, the most can be made of the advantages of both the amorphous silicon film, through which current does not flow easily, and the crystalline silicon film, through which current easily flows.

Next, as shown in Fig. 3B, a protecting film 303 is formed on the crystalline silicon film 302 from a silicon oxide film having a thickness of 130 nm. This thickness may be chosen within the range of 100 to 200 nm (preferably between 130 and 170 nm). Furthermore, other films may also be used providing that they are insulating films containing silicon. The protecting film 303 is formed so that the crystalline silicon film is not directly exposed to plasma during addition of an impurity, and so that it is possible to have delicate concentration control of the impurity.

Resist masks 304a and 304b are then formed on the protecting film 303, and an impurity element which imparts n-type conductivity (hereafter referred to as an n-type impurity element) is added. Note that elements residing in periodic table group 15 are generally used as the n-type impurity element, and typically phosphorous or arsenic can be used. Note that a plasma doping method is used, in which phosphine (PH_3) is plasma activated without separation of mass, and phosphorous is added at a concentration of $1x10^{18}$ atoms/cm^3 in embodiment 1. An ion implantation method, in which separation of mass is performed, may also be used, of course.

The dose amount is regulated so that the n-type impurity element is contained in n-type impurity regions 305 and 306, thus formed by this process, at a concentration of $2x10^{16}$ to $5x10^{19}$ atoms/cm^3 (typically between $5x10^{17}$ and $5x10^{18}$ atoms/cm^3).

Next, as shown in Fig. 3C, the protecting film 303 is removed, and activation

of the added periodic table group 15 element is performed. A known technique of activation may be used as the means of activation, and activation is done in embodiment 1 by irradiation of excimer laser light. Both of pulse emission type laser and a continuous emission type laser may be used, and it is not necessary to place any limits on the use of excimer laser light. The goal is the activation of the added impurity element, and it is preferable that irradiation is performed at an energy level at which the crystalline silicon film does not melt. Note that the laser irradiation may also be performed with the protecting film 303 in place.

Activation by heat treatment may also be performed along with activation of the impurity element by laser light. When activation is performed by heat treatment, considering the heat resistance of the substrate, it is good to perform heat treatment on the order of 450 to 550° C.

A boundary portion (connecting portion) with regions along the edges of the n-type impurity regions 305 and 306, namely regions along the perimeter into which the n-type impurity element, which exists in the n-type impurity regions 305 and 306, is not added, is delineated by this process. This means that, at the point when the TFTs are later completed, extremely good connections can be formed between LDD regions and channel forming regions.

Unnecessary portions of the crystalline silicon film are removed next, as shown in Fig. 3D, and island shape semiconductor films (hereafter referred to as active layers) 307 to 310 are formed.

Then, as shown in Fig. 3E, a gate insulating film 311 is formed, covering the active layers 307 to 310. An insulating film containing silicon and with a thickness of 10 to 200 nm, preferably between 50 and 150 nm, may be used as

the gate insulating film 311. A single layer structure or a lamination structure may be used. A 110 nm thick silicon oxynitride film is used in embodiment 1.

A conducting film with a thickness of 200 to 400 nm is formed next and patterned, forming gate electrodes 312 to 316. Note that in embodiment 1, the gate electrodes and lead wirings electrically connected to the gate electrodes (hereafter referred to as gate wirings) are formed from different materials. Specifically, a material having a lower resistance than that of the gate electrodes is used for the gate wirings. This is because a material which is capable of being micro-processed is used as the gate electrodes, and even if the gate wirings cannot be micro-processed, the material used for the wirings has low resistance. Of course, the gate electrodes and the gate wirings may also be formed from the same material.

Further, the gate wirings may be formed by a single layer conducting film, and when necessary, it is preferable to use a two layer or a three layer lamination film. All known conducting films can be used as the gate electrode material. However, as stated above, it is preferable to use a material which is capable of being micro-processed, specifically, a material which is capable of being patterned to a line width of 2 μm or less.

Typically, a film of a material chosen from among the group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), and chromium (Cr); or a nitrated compound of the above elements (typically a tantalum nitride film, a tungsten nitride film, or a titanium nitride film); or an alloy film of a combination of the above elements (typically a Mo-W alloy or a Mo-Ta alloy); or a silicide film of the above elements (typically a tungsten silicide film or a titanium silicide film); or a silicon film which has been made to possess

conductivity can be used. A single layer film or a lamination may be used, of course.

A lamination film made from a 50 nm thick tantalum nitride (TaN) film and a 350 nm thick Ta film is used in embodiment 1. It is good to form this film by sputtering. Furthermore, if an inert gas such as Xe or Ne is added as a sputtering gas, then film peeling due to the stress can be prevented.

The gate electrodes 313 and 316 are formed at this time so as to overlap a portion of the n-type impurity regions 305 and 306, respectively, sandwiching the gate insulating film 311. This overlapping portion later becomes an LDD region overlapping the gate electrode.

Next, an n-type impurity element (phosphorous is used in embodiment 1) is added in a self-aligning manner with the gate electrodes 312 to 316 as masks, as shown in Fig. 4A. The addition is regulated so that phosphorous is added to impurity regions 317 to 323 thus formed at a concentration of 1/10 to 1/2 that of the impurity regions 305 and 306 (typically between 1/4 and 1/3). Specifically, a concentration of $1x10^{16}$ to $5x10^{18}$ atoms/cm^3 (typically $3x10^{17}$ to $3x10^{18}$ atoms/cm^3) is preferable.

Resist masks 324a to 324d are formed next to cover the gate electrodes, as shown in Fig. 4B, and an n-type impurity element (phosphorous is used in embodiment 1) is added, forming impurity regions 325 to 331 containing a high concentration of phosphorous. Ion doping using phosphine (PH_3) is also performed here, and is regulated so that the phosphorous concentration of these regions is from $1x10^{20}$ to $1x10^{21}$ atoms/cm^3 (typically between $2x10^{20}$ and $5x10^{20}$ atoms/cm^3).

A source region or a drain region of the n-channel TFT is formed by this

process, and in the switching TFT, a portion of the n-type impurity regions 320 to 322 formed by the process of Fig. 4A remains. These remaining regions correspond to the LDD regions 15a to 15d of the switching TFT in Fig. 1.

Next, as shown in Fig. 4C, the resist masks 324a to 324d are removed, and a new resist mask 332 is formed. A p-type impurity element (boron is used in embodiment 1) is then added, forming impurity regions 333 and 334 containing a high concentration of boron. Boron is added here to a concentration of $3x10^{20}$ to $3x10^{21}$ atoms/cm^3 (typically between $5x10^{20}$ and $1x10^{21}$ atoms/cm^3) by ion doping using diborane (B_2H_6).

Note that phosphorous has already been added to the impurity regions 333 and 334 at a concentration of $1x10^{16}$ to $5x10^{18}$ atoms/cm^3, but boron is added here at a concentration of at least 3 times that of the phosphorous. Therefore, the n-type impurity regions already formed completely invert to p-type, and function as p-type impurity regions.

Next, after removing the resist mask 332, the n-type and p-type impurity elements added at various concentrations are activated. Furnace annealing, laser annealing, or lamp annealing may be performed as a means of activation. Heat treatment is performed in embodiment 1 in a nitrogen atmosphere for 4 hours at 550°C in an electric furnace.

It is important to remove as much of the oxygen in the atmosphere as possible at this time. This is because if any oxygen exists, then the exposed surface of the electrode oxidizes, inviting an increase in resistance, and at the same time it becomes more difficult to later make an ohmic contact. It is therefore preferable that the concentration of oxygen in the atmosphere in the above activation process be 1 ppm or less, desirably 0.1 ppm or less.

After the activation process is completed, a gate wiring 335 with a thickness of 300 nm is formed next. A metallic film having aluminum (Al) or copper (Cu) as its principal constituent (comprising 50 to 100% of the composition) may be used as the material of the gate wiring 335. As with the gate wiring 211 of Fig. 2, the gate wiring 335 is formed with a placement so that the gate electrodes 314 and 315 of the switching TFTs (corresponding to gate electrodes 19a and 19b of Fig. 2) are electrically connected. (See Fig. 4D.)

The wiring resistance of the gate wiring can be made extremely small by using this type of structure, and therefore a pixel display region (pixel portion) having a large surface area can be formed. Namely, the pixel structure of embodiment 1 is extremely effective because an EL display device having a screen size of a 10 inch diagonal or larger (in addition, a 30 inch or larger diagonal) is realized.

A first interlayer insulating film 336 is formed next, as shown in Fig. 5A. A single layer insulating film containing silicon is used as the first interlayer insulating film 336, but a lamination film may be combined in between. Further, a film thickness of between 400 nm and 1.5 μm may be used. A lamination structure of an 800 nm thick silicon oxide film on a 200 nm thick silicon oxynitride film is used in embodiment 1.

In addition, heat treatment is performed for 1 to 12 hours at 300 to 450° C in an atmosphere containing between 3 and 100% hydrogen, performing hydrogenation. This process is one of hydrogen termination of dangling bonds in the semiconductor film by hydrogen which is thermally activated. Plasma hydrogenation (using hydrogen activated by a plasma) may also be performed as

another means of hydrogenation.

Note that the hydrogenation step may also be inserted during the formation of the first interlayer insulating film 336. Namely, hydrogen processing may be performed as above after forming the 200 nm thick silicon oxynitride film, and then the remaining 800 nm thick silicon oxide film may be formed.

A contact hole is formed next in the first interlayer insulating film 336, and source wirings 337 to 340, and drain wirings 341 to 343 are formed. In embodiment 1, a lamination film with a three layer structure of a 100 nm titanium film, a 300 nm aluminum film containing titanium, and a 150 nm titanium film, formed successively by sputtering, is used as these wirings. Other conducting films may also be used, of course, and an alloy film containing silver, palladium, and copper may also be used.

A first passivation film 344 is formed next with a thickness of 50 to 500 nm (typically between 200 and 300 nm). A 300 nm thick silicon oxynitride film is used as the first passivation film 344 in embodiment 1. This may also be substituted by a silicon nitride film. It is of course possible to use the same materials as those of the first passivation film 41 of Fig. 1.

Note that it is effective to perform plasma processing using a gas containing hydrogen such as H_2 or NH_3 before the formation of the silicon oxynitride film. Hydrogen activated by this preprocess is supplied to the first interlayer insulating film 336, and the film quality of the first passivation film 344 is improved by performing heat treatment. At the same time, the hydrogen added to the first interlayer insulating film 336 diffuses to the lower side, and the active layers can be hydrogenated effectively.

Next, as shown in Fig. 5B, a color filter 345 and a fluorescing body 346

are formed. Known materials may be used for these. Furthermore, they may be formed by being patterned separately, or they may be formed in succession and then patterned together. A method such as screen printing, ink jetting, or mask evaporation (a selective forming method using a mask material) may be used as the formation method.

The respective film thickness may be chosen in the range of 0.5 to 5 μm (typically between 1 and 2 μm). In particular, the optimal film thickness of the fluorescing body 346 varies with the material used. In other words, if it is too thin, then the color transformation efficiency becomes poor, and if it is too thick, then the step becomes large and the amount of light transmitted drops. Optimal film thicknesses must therefore be set by taking a balance of both characteristics.

Note that, in embodiment 1, an example of a color changing method in which the light emitted from the EL layer is transformed in color, but if a method of manufacturing individual EL layers which correspond to R, G, and B, is employed, then the color filter and the fluorescing body can be omitted.

A second interlayer insulating film 347 is formed next from an organic resin. Materials such as polyimide, polyamide, acrylic, and BCB (benzocyclobutene) can be used as the organic resin. In particular, the purpose of being a leveling film is strong in the second interlayer insulating film 347, and therefore acrylic, having superior leveling characteristics, is preferable. An acrylic film is formed in embodiment 1 with a film thickness which can sufficiently level the step between the color filter 345 and the fluorescing body 346. This thickness is preferably from 1 to 5 μm (more preferably between 2 and 4 μm).

A contact hole for reaching the drain wiring 343 is formed next in the second

interlayer insulating film 347 and in the first passivation film 344, and a pixel electrode 348 is formed. A compound of indium oxide and tin oxide is formed into 110 nm thick in embodiment 1, and patterning is performed, making the pixel electrode. The pixel electrode 348 becomes an anode of the EL element. Note that it is also possible to use other materials: a compound film of indium oxide and zinc oxide, or a zinc oxide film containing gallium oxide.

Note that embodiment 1 becomes a structure in which the pixel electrode 348 is electrically connected to the drain region 331 of the current control TFT, through the drain wiring 343. This structure has the following advantages.

The pixel electrode 348 becomes directly connected to an organic material such as the EL layer (emitting layer) or a charge transporting layer, and therefore it is possible for the mobile ions contained in the EL layer to diffuse throughout the pixel electrode. In other words, without connecting the pixel electrode 348 directly to the drain region 331, a portion of the active layer, the introduction of mobile ions into the active layer due to the drain wiring 343 being interrupted can be prevented in the structure of embodiment 1.

Next, as shown in Fig. 5C, an EL layer 349, a cathode (MgAg electrode) 350, and a protecting electrode 351 are formed in succession without exposure to the atmosphere. It is preferable, at this point, to perform heat treatment of the pixel electrode 348, completely removing all moisture, before forming the EL layer 349 and the cathode 350. Note that a known material can be used as the EL layer 349.

The materials explained in the "embodiment mode" section of this specification can be used as the EL layer 349. In embodiment 1, an EL layer having a 4 layer structure of a hole injecting layer, a hole transporting layer,

an emitting layer, and an electron transporting layer is used, as shown in Fig. 19, but there are cases in which the electron transporting layer is not formed, and cases in which an electron injecting layer is also formed. Furthermore, there are also cases in which the hole injecting layer is omitted. Several examples of these types of combinations have already been reported, and any of these constitutions may be used.

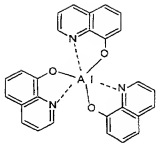
An amine such as TPD (triphenylamine dielectric) may be used as the hole injecting layer or as the hole transporting layer, and in addition, a hydrazone (typically DEH), a stilbene(typically STB), or a starburst (typically m-MTDATA) can also be used. In particular, a starburst material, which has a high glass transition temperature and is difficult to crystallize, is preferable. Further, polyaniline (PAni), polythiophene (PEDOT), and copper phthalocyanine (CuPc) may also be used.

BPPC, perylene, and DCM can be used as a red color emitting layer in the emitting layer, and in particular, the Eu complex shown by $Eu(DBM)_3(Phen)$ (refer to Kido, J., et. al, Appl. Phys., vol. 35, pp. L394-6, 1996 for details) is highly monochromatic, possessing a sharp emission at a wavelength of 620 nm.

Further, typically an Alq_3 (8-hydroxyquinoline aluminum) material in which quinacridone or coumarin is added at a level of several mol% can be used as a green color emitting layer.

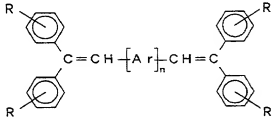
The chemical formula is as shown below.

[formula 6]



In addition, typically a distile-arylene amino dielectric, in which amino substituted DSA is added to DSA (distile-arylene dielectric) can be used as a blue color emitting layer. In particular, it is preferable to use the high performance material distilyl-biphenyl (DPVBi). Its chemical formula is as shown below.

[formula 7]



Further, a 300 nm thick silicon nitride film is formed as a second passivation film 352, and this may also be formed in succession, without exposure to the atmosphere, after formation of the protecting electrode 351. The same materials as those of the second passivation film 49 of Fig. 1 can also be used, of course, as the second passivation film 352.

A 4 layer structure made from a hole injecting layer, a hole transporting layer, an emitting layer, and an electron injecting layer is used in embodiment 1, but there are already examples of many combinations already reported, and any of these constitutions may also be used. Furthermore, an MgAg electrode

is used as the cathode of the EL element in embodiment 1, but other known materials may also be used.

The protecting electrode 351 is formed in order to prevent deterioration of the MgAg electrode 350, and a metallic film having aluminum as its principal constituent is typical. Other materials may, of course, also be used. Furthermore, the EL layer 349 and the MgAg electrode 350 are extremely weak with respect to moisture, and therefore it is preferable to perform successive formation up through to the protecting electrode 351 without exposure to the atmosphere, protecting the EL layer from external air.

Note that the film thickness of the EL layer 349 may be from 10 to 400 nm (typically between 60 and 160 nm), and that the thickness of the MgAg electrode 350 may be from 180 to 300 nm (typically between 200 and 250 nm).

The active matrix type EL display device with the structure shown in Fig. 5C is thus completed. By arranging TFTs with optimal structure in not only the pixel portion, but also in the driver circuit portion, the active matrix type EL display device of embodiment 1 shows extremely high reliability, and the operational characteristics can be raised.

First, a TFT having a structure which reduces hot carrier injection as much as possible without a drop in the operation speed is used as an n-channel TFT 205 of the CMOS circuit forming the driver circuits. Note that the driver circuits referred to here include circuits such as a shift register, a buffer, a level shifter, and a sampling circuit (also referred to as a transfer gate). When digital driving is performed, signal conversion circuits such as a D/A converter circuit are also included.

In the case of embodiment 1, an active layer of the n-channel TFT 205

includes a source region 355, a drain region 356, an LDD region 357, and a channel forming region 358, as shown in Fig. 5C, and the LDD region 357 overlaps the gate electrode 313, sandwiching the gate insulating film 311.

The formation of the LDD region on the drain side only is in consideration of not lowering the operation speed. Further, it is not necessary to be concerned with the value of the off current in the n-channel TFT 205, and greater emphasis may be placed on the operation speed. It is therefore preferable that the LDD region 357 completely overlap the gate electrode 313, reducing resistive components as much as possible. In other words, it is good to eliminate all offset.

Deterioration of a p-channel TFT 206 of the CMOS circuit due to hot carrier injection is almost of no concern, and in particular, therefore, an LDD region is not formed. It is also possible, of course, to take action against hot carriers by forming an LDD region similar to that of the n-channel TFT 205.

Note that among the driver circuits, the sampling circuit is somewhat special when compared to the other circuits, and a large current flows in the channel forming region in both directions. Namely, the roles of the source region and the drain region change. In addition, it is necessary to suppress the value of the off current as much as possible, and with that in mind, it is preferable to arrange a TFT having functions at an intermediate level between the switching TFT and the current control TFT.

It is preferable, therefore, to arrange a TFT with the structure shown in Fig. 9 as an n-type TFT forming the sampling circuit. As shown in Fig. 9, a portion of LDD regions 901a and 901b overlap a gate electrode 903, sandwiching a gate insulating film 902. This effect is as stated in the explanation of the

current control TFT 202, and the case of the sampling circuit differs in the point of forming the LDD regions 901a and 901b with a shape that sandwiches a channel forming region 904.

Further, a pixel with the structure shown in Fig. 1 is formed, forming a pixel portion. The structures of a switching TFT and a current control TFT formed within the pixel have already been explained in Fig. 1, and therefore that explanation is omitted here.

Note that, in practice, it is preferable to additionally perform packaging (sealing) after completing up through Fig. 5C by using a housing material such as a highly airtight protecting film (such as a laminar film or an ultraviolet hardened resin film) or a ceramic sealing can, so that there is no exposure to the atmosphere. By making the inside of the housing material an inert environment, and by placing an absorbing agent (for example, barium oxide) within the housing material, the reliability (life) of the EL layer is increased.

Furthermore, after the airtightness is increased by the packaging processing, a connector (a flexible printed circuit, FPC) for connecting between output terminals from elements or circuits formed on the substrate, and external signal terminals, is attached, completing a manufactured product. The EL display device in this state of being able to be shipped is referred to as an EL module throughout this specification.

The constitution of the active matrix type EL display device of embodiment 1 is explained here using the perspective view of Fig. 6. The active matrix type EL display device of embodiment 1 is formed on a glass substrate 601, and is composed of a pixel portion 602, a gate side driving circuit 603, and a source side driving circuit 604. A switching TFT 605 of the pixel portion is an

n-channel TFT, and is placed at the intersection of a gate wiring 606 connected to the gate side driving circuit 603, and a source wiring 607 of the source side driving circuit 604. Furthermore, the drain of the switching TFT 605 is electrically connected to the gate of a current control TFT 608.

In addition, the source of the current control TFT 608 is connected to a current supply line 609, and an EL element 610 is electrically connected to the drain of the current control TFT 608. Provided that the current control TFT 608 is an n-channel TFT, it is preferable to connect the cathode of the EL element 610 to the drain of the current control TFT 608 at this point. Further, if the current control TFT 608 is a p-channel TFT, then it is preferable to connect the anode of the EL element 610 to the drain of the current control TFT 608.

Input wirings (connection wirings) 612 and 613, and an input wiring 614 which is connected to the current supply line 609, are then formed in an external input terminal FPC 611 in order to transfer signals to the driver circuits.

Shown in Fig. 7 is one example of the circuit composition of the EL display device shown in Fig. 6. The EL display device of embodiment 1 has a source side driving circuit 701, a gate side driving circuit (A) 707, a gate side driving circuit (B) 711, and a pixel portion 706. Note that, throughout this specification, driver circuit is a generic term which includes source side processing circuits and gate side processing circuits.

The source side driving circuit 701 is provided with a shift register 702, a level shifter 703, a buffer 704, and a sampling circuit (transfer gate) 705. In addition, the gate side driving circuit (A) 707 is provided with a shift register 708, a level shifter 709, and a buffer 710. The gate side driving circuit (B) 711 has a similar composition.

The driving voltage is from 5 to 16 V (typically 10 V) for the shifter registers 702 and 708 here, and the structure shown by reference numeral 205 of Fig. 5C is suitable for an n-channel TFT used in a CMOS circuit forming the circuits.

Furthermore, the driving voltage becomes high at between 14 and 16 V for the level shifters 703 and 709, and for the buffers 704 and 710, and similar to the shifters, a CMOS circuit containing the n-channel TFT 205 of Fig. 5C is suitable. Note that the use of a multi-gate structure, such as a double gate structure or a triple gate structure for the gate wirings, is effective by increasing the reliability of each circuit.

The driving voltage is between 14 and 16 V for the sampling circuit 705, but it is necessary to reduce the value of the off current because the source region and the drain region invert, and therefore a CMOS circuit containing the n-channel TFT 208 of Fig. 9 is suitable.

In addition, the driving voltage of the pixel portion 706 is between 14 and 16 V, and a pixel with the structure shown in Fig. 1 is arranged.

Note that the above constitutions can be easily realized by manufacturing TFTs in accordance with the manufacturing processes shown in Figs. 3A to 5C. Furthermore, only the constitution of the pixel portion and the driver circuits is shown in embodiment 1, but it is also possible to form other logic circuits, in addition to the driving circuits, on the same substrate and in accordance with the manufacturing process of embodiment 1, such as a signal divider circuit, a D/A converter circuit, an op-amp circuit, and a γ compensation circuit. In addition, it is considered that circuits such as a memory portion and a microprocessor can also be formed.

An explanation of the EL module of embodiment 1, containing the housing material, is made using Figs. 17A and 17B. Note that, when necessary, the symbols used in Figs. 6 and 7 are cited.

A pixel portion 1701, a source side driving circuit 1702, and a gate side driving circuit 1703 are formed on a substrate (including a base film underneath a TFT) 1700. Various wirings from the respective driver circuits are connected to external equipment, via the FPC 611, through the input wirings 612 to 614.

A housing material 1704 is formed at this point enclosing at least the pixel portion, and preferably the driving circuits and the pixel portion. Note that the housing material 1704 is of an irregular shape in which the internal size is larger than the external size of the EL element, or has a sheet shape, and is fixed to the substrate 1700 by an adhesive 1705 so as to form an airtight space jointly with the substrate 1700. At this point, the EL element is in a state of being completely sealed in the above airtight space, and is completely cutoff from the external atmosphere. Note that a multiple number of housing materials 1704 may be formed.

It is preferable to use an insulating substance such as a glass or a polymer as the housing material 1704. The following can be given as examples: amorphous glass (such as borosilicate glass or quartz); crystallized glass; ceramic glass; organic resins (such as acrylic resins, styrene resins, polycarbonate resins, and epoxy resins); and silicone resins. In addition, ceramics may also be used. Furthermore, provided that the adhesive 1705 is an insulating material, it is also possible to use a metallic material such as a stainless alloy.

It is possible to use an adhesive such as an epoxy resin or an acrylate resin as the material of the adhesive 1705. In addition, a thermally hardened

resin or a light hardened resin can also be used as the adhesive. Note that it is necessary to use a material through which, as much as is possible, oxygen and moisture is not transmitted.

In addition, it is preferable to fill an opening 1706 between the housing material and the substrate 1700 with an inert gas (such as argon, helium, or nitrogen). There are no limitations on a gas, and it is also possible to use an inert liquid (such as a liquid fluorinated carbon, typically perfluoroalkane). The materials such as those used by Japanese Patent Application Laid-open No. Hei 8-78519 may be referred to regarding inert liquids. The space may also be filled with a resin.

It is effective to form drying agent in the opening 1706. Materials such as those recorded in Japanese Patent Application Laid-open No. Hei 9-148066 can be used as the drying agent. Typically, barium oxide may be used. Furthermore, it is effective to form an antioxidizing agent as well, not just a drying agent.

A plural number of isolated pixels having EL elements are formed in the pixel portion, as shown in Fig. 17B, and all of the pixels have a protecting electrode 1707 as a common electrode. In embodiment 1 it is preferable to form the EL layer, the cathode (MgAg electrode), and the protecting electrode in succession, without exposure to the atmosphere. The EL layer and the cathode are formed using the same mask material, and provided that only the protecting electrode is formed by a separate mask material, then the structure of Fig. 17B can be realized.

The EL layer and the cathode may be formed only in the pixel portion at this point, and it is not necessary to form them on the driving circuits. There is no problem, of course, with forming them on the driving circuits, but

considering the fact that alkaline metals are contained in the EL layer, it is preferable to not form it over the driving circuits.

Note that an input wiring 1709 is connected to the protecting electrode 1707 in a region shown by reference numeral 1708. The input wiring 1709 is a wiring for providing a preset voltage to the protecting electrode 1707, and is connected to the FPC 611 through a conducting paste material (typically an anisotropic conducting film) 1710.

A manufacturing process for realizing a contact structure in the region 1708 is explained here using Figs. 18A to 18C.

First, the state of Fig. 5A is obtained in accordance with the processes of embodiment 1. At this point the first interlayer insulating film 336 and the gate insulating film 311 are removed from the edges of the substrate (in the region shown by reference numeral 1708 in Fig. 17B), and the input wiring 1709 is formed on that region. The source wirings and the drain wirings of Fig. 5A are of course formed at the same time. (See Fig. 18A.)

Next, when etching the second interlayer insulating film 347 and the first passivation film 344 in Fig. 5B, a region shown by reference numeral 1801 is removed, and an open portion 1802 is formed. (See Fig. 18B.)

The processes of forming the EL element (pixel electrode, EL layer, and cathode formation processes) in the pixel portion are performed in this state. A mask material is used in the region shown in Figs. 18A to 18C at this time so that the EL element is not formed in this region. After forming the cathode 349, the protecting electrode 350 is formed using a separate mask material. The protecting electrode 350 and the input wiring 1709 are thus electrically connected. Further, the second passivation film 352 is formed, and the state

of Fig. 18C is obtained.

The contact structure of the region shown by reference numeral 1708 in Fig. 17B is thus realized by the above steps. The input wiring 1709 is then connected to the FPC 611 through the opening between the housing material 1704 and the substrate 1700 (note that this is filled by the adhesive 1705; in other words, it is necessary for the thickness of the adhesive 1705 to be such that it can sufficiently level the step of the input wiring). Note that an explanation of the input wiring 1709 is made here, but the other input wirings 612 to 614 are also similarly connected to the FPC 611 by passing under the housing material 1704.

Embodiment 2

In embodiment 2, an example of a pixel constitution is shown in Fig. 10 which differs from the constitution shown in Fig. 2B.

The two pixels shown in Fig. 2B are arranged with symmetry around the current supply line in embodiment 2. Namely, as shown in Fig. 10, by making the current supply line 213 common between the two pixels neighboring the current supply line, the number of wirings needed can be reduced. Note that the structure of the TFTs placed inside the pixels may be left as is.

If this type of constitution is used, then it becomes possible to manufacture a very high definition pixel portion, increasing the image quality.

Note that the constitution of embodiment 2 can easily be realized in accordance with the manufacturing processes of embodiment 1, and that the explanations of embodiment 1 and of Fig. 1 may be referenced regarding points

such as the structure of the TFTs.

Embodiment 3

A case of forming a pixel portion having a structure which differs from that of Fig. 1 is explained using Fig. 11 in embodiment 3. Note that processes up through the formation of the second interlayer insulating film 44 may be performed in accordance with embodiment 1. Furthermore, the structures of the switching TFT 201 and the current control TFT 202, covered by the second interlayer insulating film 44, are the same as those of Fig. 1, and their explanation is therefore omitted.

In the case of embodiment 3, a pixel electrode 51, a cathode 52, and an EL layer 53 are formed after forming a contact hole in the second interlayer insulating film 44 and the first passivation film 41. The cathode 52 and the EL layer 53 are formed in succession, without exposure to the atmosphere, by vacuum evaporation in embodiment 3, and at that time a red color emitting EL layer, a green color emitting EL layer, and a blue color emitting layer are formed selectively in separate pixels by using a mask material. Note that while only one pixel is shown in Fig. 11, pixels with the same structure are formed corresponding to the colors of red, green, and blue, respectively, and that color display can be performed by these pixels. A known material may be employed for each EL layer color.

A 150 nm thick aluminum alloy film (an aluminum film containing 1 wt% of titanium) is formed as the pixel electrode 51 in embodiment 3. Provided that it is a metallic material, any material may be used as the pixel electrode material, but it is preferable to use a material having a high reflectivity.

Further, a 230 nm thick MgAg electrode is used as the cathode 52, and the film thickness of the EL layer 53 is 90 nm (including, from the bottom, a 20 nm electron transporting layer, a 40 nm emitting layer, and a 30 nm hole transporting layer).

An anode 54 made from a transparent conducting film (an ITO film in embodiment 3) is formed next with a thickness of 110 nm. An EL element 209 is thus formed, and if a second passivation film 55 is formed by the same materials as shown in embodiment 1, then a pixel with the structure shown in Fig. 11 is completed.

When using the structure of embodiment 3, the red, green, or blue light generated by each pixel is irradiated in the opposite direction as that of the substrate on which the TFTs are formed. For that reason, almost the entire area inside the pixel, namely the region in which the TFTs are formed, can be used as an effective emitting region. As a result, there is a sharp increase in the effective emitting surface area of the pixel, and the brightness and the contrast ratio (the ratio between light and dark) of the image are increased.

Note that it is possible to freely combine the composition of embodiment 3 with the constitutions of any of embodiments 1 and 2.

Embodiment 4

A case of forming a pixel having a structure which differs from that of Fig. 2 of embodiment 1 is explained in embodiment 4 using Figs. 12A and 12B.

In Fig. 12A, reference numeral 1201 denotes a switching TFT, which comprises an active layer 56, a gate electrode 57a, a gate wiring 57b, a source wiring 58, and a drain wiring 59. Further, reference numeral 1202 denotes a current

control TFT, which comprises an active layer 60, a gate electrode 61, a source wiring 62, and a drain wiring 63. The source wiring 62 of the current control TFT 1202 is connected to a current supply line 64, and the drain wiring 63 is connected to an EL element 65. Fig. 12B shows the circuit composition of this pixel.

The point of difference between Fig. 12A and Fig. 2A is the structure of the switching TFT. In embodiment 4 the gate electrode 57a is formed with a fine line width between 0.1 and 5 μm, and the active layer 56 is formed so as transverse that portion. The gate wiring 57b is formed so as to electrically connect the gate electrode 57a of each pixel. A triple gate structure which does not monopolize much surface area is thus realized.

Other portions are similar to those of Fig. 2A, and the effective emitting surface area becomes larger because the surface area exclusively used by the switching TFT becomes smaller if the structure of embodiment 4 is employed. In other words, the image brightness is increased. Furthermore, a gate structure in which redundancy is increased in order to reduce the value of the off current can be realized, and therefore the image quality can be increased even further.

Note that, in the constitution of embodiment 4, the current supply line 64 can be made common between neighboring pixels, as in embodiment 2, and that a structure like that of embodiment 3 may also be used. Furthermore, processes of manufacturing may be performed in accordance with those of embodiment 1.

Embodiment 5

Cases in which a top gate type TFT is used are explained in embodiments

1 to 4, and the present invention may also be implemented using a bottom gate type TFT. A case of implementing the present invention by using a reverse stagger type TFT is explained in embodiment 5 using Fig. 13. Note that, except for the structure of the TFT, the structure is the same as that of Fig. 1, and therefore the same symbols as those of Fig. 1 are used when necessary.

In Fig. 13, the similar materials as those of Fig. 1 can be used in the substrate 11 and in the base film 12. A switching TFT 1301 and a current control TFT 1302 are then formed on the base film 12.

The switching TFT 1301 comprises: gate electrodes 70a and 70b; a gate wiring 71; a gate insulating film 72; a source region 73; a drain region 74; LDD regions 75a to 75d; a high concentration impurity region 76; channel forming regions 77a and 77b; channel protecting films 78a and 78b; a first interlayer insulating film 79; a source wiring 80; and a drain wiring 81.

Further, the current control TFT 1302 comprises: a gate electrode 82; the gate insulating film 72; a source region 83; a drain region 84; an LDD region 85; a channel forming region 86; a channel protecting film 87; a first interlayer insulating film 79; a source wiring 88; and a drain wiring 89. The gate electrode 82 is electrically connected to the drain wiring 81 of the switching TFT 1301 at this point.

Note that the above switching TFT 1301 and the current control TFT 1302 may be formed in accordance with a known method of manufacturing a reverse stagger type TFT. Further, similar materials used in corresponding portions of the top gate type TFTs of embodiment 1 can be used for the materials of each portion (such as wirings, insulating films, and active layers) formed in the above TFTs. Note that the channel protecting films 78a, 78b, and 87, which are not in the

constitution of the top gate type TFT, may be formed by an insulating film containing silicon. Furthermore, regarding the formation of impurity regions such as the source regions, the drain regions, and the LDD regions, they may be formed by using a photolithography technique and individually changing the impurity concentration.

When the TFTs are completed, a pixel having an EL element 1303 in which the first passivation film 41, the insulating film (leveling film) 44, the second passivation film 49, the pixel electrode (anode) 46, the EL layer 47, the MgAg electrode (cathode) 45, the aluminum electrode (protecting film) 48, and the third passivation film 50 are formed in order, is completed. Embodiment 1 may be referred to with respect to manufacturing processes and materials for the above.

Note that it is possible to freely combine the constitution of embodiment 5 with the constitution of any of embodiments 2 to 4.

Embodiment 6

It is effective to use a material having a high thermal radiating effect, similar to that of the first passivation film 41 and the second passivation film 49, as the base film formed between the active layer and the substrate in the structures of Fig. 5C of embodiment 1 or Fig. 1. In particular, a large amount of current flows in the current control TFT, and therefore heat is easily generated, and deterioration due to self generation of heat can become a problem. Thermal deterioration of the TFT can be prevented by using the base film of embodiment 6, which has a thermal radiating effect, for this type of case.

The effect of protecting from the diffusion of mobile ions from the substrate is also very important, of course, and therefore it is preferable to use a lamination structure of a compound including Si, Al, N, O, and M, and an insulating film containing silicon, similar to the first passivation film 41.

Note that it is possible to freely combine the constitution of embodiment 6 with the constitution of any of embodiments 1 to 5.

Embodiment 7

When the pixel structure shown in embodiment 3 is used, the light emitted from the EL layer is radiated in the direction opposite to the substrate, and therefore it is not necessary to pay attention to the transmissivity of materials, such as the insulating film, which exist between the substrate and the pixel electrode. In other words, materials which have a somewhat low transmissivity can also be used.

It is therefore advantageous to use a carbon film, such as one referred to as a diamond thin film, a diamond-like carbon film, or an amorphous carbon film, as the base film 12 or the first passivation film 41. In other words, because it is not necessary to worry about lowering the transmissivity, the film thickness can be set thick, to between 100 and 500 nm, and it is possible to have a very high thermal radiating effect.

Regarding the use of the above carbon films in the second passivation film 49, note that a reduction in the transmissivity must be avoided, and therefore it is preferable to set the film thickness to between 5 and 100 nm.

Note that, in embodiment 7, it is effective to laminate with another

insulating film when a carbon film is used in any of the base film 12, the first passivation film 41 and the second passivation film 49.

In addition, embodiment 7 is effective when the pixel structure shown in embodiment 3 is used, and for other constitutions, it is possible to freely combine the constitution of embodiment 7 with the constitution of any of embodiments 1 to 6.

Embodiment 8

The amount of the off current value in the switching TFT in the pixel of the EL display device is reduced by using a multi-gate structure for the switching TFT, and the present invention is characterized by the elimination of the need for a storage capacitor. This is a device for making good use of the surface area, reserved for the storage capacitor, as an emitting region.

However, even if the storage capacitor is not completely eliminated, an effect of increasing the effective emitting surface area, by the amount that the exclusive surface area is made smaller, can be obtained. In other words, the object of the present invention can be sufficiently achieved by reducing the value of the off current by using a multi-gate structure for the switching TFT, and by only shrinking the exclusive surface area of the storage capacitor.

It is therefore possible to use a pixel structure such as that shown in Fig. 14. Note that, when necessary, the same symbols are used in Fig. 14 as in Fig. 1.

The different point between Fig. 14 and Fig. 1 is the existence of a storage capacitor 1401 connected to the switching TFT. The storage capacitor 1401 is

formed by a semiconductor region (lower electrode) extended from the drain region 14 of the switching TFT 201, the gate insulating film 18, and a capacitor electrode (upper electrode) 1403. The capacitor electrode 1403 is formed at the same time as the gate electrodes 19a, 19b, and 35 of the TFT.

A top view is shown in Fig. 15A. The cross sectional diagram taken along the line A-A' in the top view of Fig. 15A corresponds to Fig. 14. As shown in Fig. 15A, the capacitor electrode 1403 is electrically connected to the source region 31 of the current control TFT through a connecting wiring 1404 which is electrically connected to the capacitor electrode 1403. Note that the connection wiring 1404 is formed at the same time as the source wirings 21 and 36, and the drain wirings 22 and 37. Furthermore, Fig. 15B shows the circuit constitution of the top view shown in Fig. 15A.

Note that the constitution of embodiment 8 can be freely combined with the constitution of any of embodiments 1 to 7. In other words, only the storage capacitor is formed within the pixel, no limitations are added with regard to the TFT structure or the EL layer materials.

Embodiment 9

Laser crystallization is used as the means of forming the crystalline silicon film 302 in embodiment 1, and a case of using a different means of crystallization is explained in embodiment 9.

After forming an amorphous silicon film in embodiment 9, crystallization is performed using the technique recorded in Japanese Patent Application Laid-open No. Hei 7-130652. The technique recorded in the above patent

application is one of obtaining a crystalline silicon film having good crystallinity by using an element such as nickel as a catalyst for promoting crystallization.

Further, after the crystallization process is completed, a process of removing the catalyst used in the crystallization may be performed. In this case, the catalyst may be gettered using the technique recorded in Japanese Patent Application Laid-open No. Hei 10-270363 or Japanese Patent Application Laid-open No. Hei 8-330602.

In addition, a TFT may be formed using the technique recorded in the specification of Japanese Patent Application Laid-open No. Hei 11-076967 by the applicant of the present invention.

The processes of manufacturing shown in embodiment 1 are one embodiment of the present invention, and provided that the structure of Fig. 1 or of Fig. 5C of embodiment 1 can be realized, then other manufacturing process may also be used without any problems, as above.

Note that it is possible to freely combine the constitution of embodiment 9 with the constitution of any of embodiments 1 to 8.

Embodiment 10

In driving the EL display device of the present invention, analog driving can be performed using an analog signal as an image signal, and digital driving can be performed using a digital signal.

When analog driving is performed, the analog signal is sent to a source wiring of a switching TFT, and the analog signal, which contains gray scale

information, becomes the gate voltage of a current control TFT. The current flowing in an EL element is then controlled by the current control TFT, the EL element emitting intensity is controlled, and gray scale display is performed. In this case, it is preferable to operate the current control TFT in a saturation region. In other words, it is preferable to operate the TFT within the conditions of $|V_{ds}| > |V_{gs} - V_{th}|$. Note that V_{ds} is the voltage difference between a source region and a drain region, V_{gs} is the voltage difference between the source region and a gate electrode, and V_{th} is the threshold voltage of the TFT.

On the other hand, when digital driving is performed, it differs from the analog type gray scale display, and gray scale display is performed by time division driving (time ratio gray scale driving) or surface area ratio gray scale driving. Namely, by regulating the length of the emission time or the ratio of emitting surface area, color gray scales can be made to be seen visually as changing. In this case, it is preferable to operate the current control TFT in the linear region. In other words, it is preferable to operate the TFT within the conditions of $|V_{ds}| < |V_{gs} - V_{th}|$.

The EL element has an extremely fast response speed in comparison to a liquid crystal element, and therefore it is possible to have high speed driving. Therefore, the EL element is one which is suitable for time ratio gray scale driving, in which one frame is partitioned into a plural number of subframes and then gray scale display is performed. Furthermore, it has the advantage of the period of one frame being short, and therefore the amount of time for which the gate voltage of the current control TFT is maintained is also short, and a storage capacitor can be made smaller or eliminated.

The present invention is a technique related to the element structure, and

therefore any method of driving it may thus be used.

Embodiment 11

In embodiment 11, examples of the pixel structure of the EL display device of the present invention are shown in Figs. 21A and 21B. Note that in embodiment 11, reference numeral 4701 denotes a source wiring of a switching TFT 4702, reference numeral 4703 denotes a gate wiring of the switching TFT 4702, reference numeral 4704 denotes a current control TFT, 4705 denotes an electric current supply line, 4706 denotes a power source control TFT, 4707 denotes a power source control gate wiring, and 4708 denotes an EL element. Japanese Patent Application Laid-open No. Hei 11-341272 may be referred to regarding the operation of the power source control TFT 4706.

Further, in embodiment 11 the power source control TFT 4706 is formed between the current control TFT 4704 and the EL element 4708, but a structure in which the current control TFT 4704 is formed between the power source control TFT 4706 and the EL element 4708 may also be used. In addition, it is preferable for the power source control TFT 4706 to have the same structure as the current control TFT 4704, or for both to be formed in series by the same active layer.

Fig. 21A is an example of a case in which the electric current supply line 4705 is common between two pixels. Namely, this is characterized in that the two pixels are formed having linear symmetry around the electric current supply line 4705. In this case, the number of electric current supply lines can be reduced, and therefore the pixel portion can be made even more high precision.

Furthermore, Fig. 21B is an example of a case in which an electric current

supply line 4710 is formed parallel to the gate wiring 4703, and in which a power source control gate wiring 4711 is formed parallel to the source wiring 4701. Note that in Fig. 23B, the structure is formed such that the electric current supply line 4710 and the gate wiring 4703 do not overlap, but provided that both are wirings formed on different layers, then they can be formed to overlap, sandwiching an insulating film. In this case, the exclusive surface area of the electric current supply line 4710 and the gate wiring 4703 can be shared, and the pixel section can be made even more high precision.

Embodiment 12

In embodiment 12, examples of the pixel structure of the EL display device of the present invention are shown in Figs. 22A and 22B. Note that in embodiment 12, reference numeral 4801 denotes a source wiring of a switching TFT 4802, reference numeral 4803 denotes a gate wiring of the switching TFT 4802, reference numeral 4804 denotes a current control TFT, 4805 denotes an electric current supply line, 4806 denotes an erasure TFT, 4807 denotes an erasure gate wiring, and 4808 denotes an EL element. Japanese Patent Application Laid-open No. Hei 11-338786 may be referred to regarding the operation of the erasure TFT 4806.

The drain of the erasure TFT 4806 is connected to a gate of the current control TFT 4804, and it becomes possible to forcibly change the gate voltage of the current control TFT 4804. Note that an n-channel TFT or a p-channel TFT may be used for the erasure TFT 4806, but it is preferable to make it the same structure as the switching TFT 4802 so that the off current value can be made smaller.

Fig. 22A is an example of a case in which the electric current supply line

4805 is common between two pixels. Namely, this is characterized in that the two pixels are formed having linear symmetry around the electric current supply line 4805. In this case, the number of electric current supply lines can be reduced, and therefore the pixel section can be made even more high precision.

In addition, Fig. 22B is an example of a case in which an electric current supply line 4810 is formed parallel to the gate wiring 4803, and in which an erasure gate wiring 4811 is formed parallel to the source wiring 4801. Note that in Fig. 22B, the structure is formed such that the electric current supply line 4810 and the gate wiring 4803 do not overlap, but provided that both are wirings formed on different layers, then they can be formed to overlap, sandwiching an insulating film. In this case, the exclusive surface area of the electric current supply line 4810 and the gate wiring 4803 can be shared, and the pixel section can be made even more high precision.

Embodiment 13

The EL display device of the present invention may have a structure in which several TFTs are formed within a pixel. In embodiments 11 and 12, examples of forming three TFTs are shown, but from 4 to 6 TFTs may also be formed. It is possible to implement the present invention without placing any limitations on the structure of the pixels of the EL display device.

Embodiment 14

An example of using a p-channel TFT as the current control TFT 202 of Fig. 1 is explained in embodiment 14. Note that other portions are the same as those

of Fig. 1, and therefore a detailed explanation of the other portions is omitted.

A cross sectional structure of the pixel of embodiment 14 is shown in Fig. 23. Embodiment 1 may be referred to for a method of manufacturing the p-channel TFT used in embodiment 14. An active layer of the p-channel TFT comprises a source region 2801, a drain region 2802, and a channel forming region 2803, and the source region 2801 is connected to the source wiring 36, and the drain region 2802 is connected to the drain wiring 37.

For cases in which the anode of an EL element is connected to the current control TFT, it is preferable to use the p-channel TFT as the current control TFT.

Note that it is possible to implement the constitution of embodiment 14 by freely combining it with the constitution of any of embodiments 1 to 13.

Embodiment 15

By using an EL material in which phosphorescence from a triplet state exciton can be utilized in light emission in embodiment 15, the external emission quantum efficiency can be increased by a great amount. By doing so, it becomes possible to make the EL element into a low power consumption, long life, and low weight EL element.

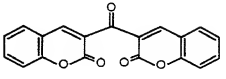
Reports of utilizing triplet state excitons and increasing the external emission quantum efficiency is shown in the following papers.

Tsutsui, T., Adachi, C., and Saito, S., Photochemical Processes in Organized Molecular Systems, Ed. Honda, K., (Elsevier Sci. Pub., Tokyo, 1991),

p. 437.

The molecular formula of the EL material (coumarin pigment) reported in the above paper is shown below.

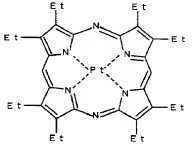
[formula 8]



Baldo, M. A., O'Brien, D. F., You, Y., Shoustikov, A., Sibley, S., Thompson, M. E., and Forrest, S. R., Nature 395 (1998) p. 151.

The molecular formula of the EL material (Pt complex) reported in the above paper is shown below.

[formula 9]



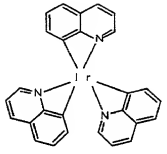
Baldo, M. A., Lamansky, S., Burrows, P. E., Thompson, M. E., and Forrest, S. R., Appl. Phys. Lett., 75 (1999) p. 4.

Tsutui, T., Yang, M. J., Yahiro, M., Nakamura, K., Watanabe, T., Tsuji, T., Fukuda, Y., Wakimoto, T., Mayaguchi, S., Jpn. Appl. Phys., 38 (12B) (1999) L1502.

The molecular formula of the EL material (Ir complex) reported in the above

paper is shown below.

[formula 10]



Provided that the phosphorescence emission from triplet state excitons can be utilized, then in principle it is possible to realize an external emission quantum efficiency which is 3 to 4 times higher than that for cases of using the fluorescence emission from singlet state excitons. Note that it is possible to implement the constitution of embodiment 15 by freely combining it with the constitution of any of embodiments 1 to 13.

Embodiment 16

In embodiment 1 it is preferable to use an organic EL material as an EL layer, but the present invention can also be implemented using an inorganic EL material. However, current inorganic EL materials have an extremely high driving voltage, and therefore a TFT which has voltage resistance characteristics that can withstand the driving voltage must be used in cases of performing analog driving.

Alternatively, if inorganic EL materials having lower driving voltages than conventional inorganic EL materials are developed, then it is possible to apply

them to the present invention.

Further, it is possible to freely combine the constitution of embodiment 16 with the constitution of any of embodiments 1 to 14.

Embodiment 17

An active matrix type EL display device (EL module) formed by implementing the present invention has superior visibility in bright locations in comparison to a liquid crystal display device because it is a self-emitting type device. It therefore has a wide range of uses as a direct-view type EL display (indicating a display incorporating an EL module).

Note that a wide viewing angle can be given as one advantage which the EL display has over a liquid crystal display. The EL display of the present invention may therefore be used as a display (display monitor) having a diagonal equal to 30 inches or greater (typically equal to 40 inches or greater) for appreciation of TV broadcasts by large screen.

Further, not only can it be used as an EL display (such as a personal computer monitor, a TV broadcast reception monitor, or an advertisement display monitor), it can be used as a display for various electronic devices.

The following can be given as examples of such electronic devices: a video camera; a digital camera; a goggle type display (head mounted display); a car navigation system; a personal computer; a portable information terminal (such as a mobile computer, a mobile telephone, or an electronic book); and an image playback device using a recording medium (specifically, a device which performs playback of a recording medium and is provided with a display which can display

those images, such as a compact disk (CD), a laser disk (LD), or a digital video disk (DVD)). Examples of these electronic devices are shown in Figs. 16A to 16F.

Fig. 16A is a personal computer, comprising a main body 2001, a casing 2002, a display portion 2003, and a keyboard 2004. The present invention can be used in the display portion 2003.

Fig. 16B is a video camera, comprising a main body 2101, a display portion 2102, an audio input portion 2103, operation switches 2104, a battery 2105, and an image receiving portion 2106. The present invention can be used in the display portion 2102.

Fig. 16C is a goggle display, comprising a main body 2201, a display portion 2202, and an arm portion 2203. The present invention can be used in the display portion 2202.

Fig. 16D is a mobile computer, comprising a main body 2301, a camera portion 2302, an image receiving portion 2303, operation switches 2304, and a display portion 2305. The present invention can be used in the display portion 2305.

Fig. 16E is an image playback device (specifically, a DVD playback device) provided with a recording medium, comprising a main body 2401, a recording medium (such as a CD, an LD, or a DVD) 2402, operation switches 2403, a display portion (a) 2404, and a display portion (b) 2405. The display portion (a) is mainly used for displaying image information, and the image portion (b) is mainly used for displaying character information, and the present invention can be used in the image portion (a) and in the image portion (b). Note that the present invention can be used as an image playback device provided with a recording medium in devices such as a CD playback device and game equipment.

Fig. 16F is an EL display, containing a casing 2501, a support stand 2502, and a display portion 2503. The present invention can be used in the display portion 2503. The EL display of the present invention is especially advantageous for cases in which the screen is made large, and is favorable for displays having a diagonal greater than or equal to 10 inches (especially one which is greater than or equal to 30 inches).

Furthermore, if the emission luminance of EL materials becomes higher in future, then it will become possible to use the present invention in a front type or a rear type projector.

The above electronic devices are becoming more often used to display information provided through an electronic transmission circuit such as the Internet or CATV (cable television), and in particular, opportunities for displaying animation information are increasing. The response speed of EL materials is extremely high, and therefore EL displays are suitable for performing this type of display.

The emitting portion of the EL display device consumes power, and therefore it is preferable to display information so as to have the emitting portion become as small as possible. Therefore, when using the EL display device in a display portion which mainly displays character information, such as a portable information terminal, in particular, a portable telephone of a car audio system, it is preferable to drive it by setting non-emitting portions as background and forming character information in emitting portions.

Fig. 20A is a portable telephone, comprising a main body 2601, an audio output portion 2602, an audio input portion 2603, a display portion 2604, operation switches 2605, and an antenna 2606. The EL display device of the

present invention can be used in the display portion 2604. Note that by displaying white characters in a black background in the display portion 2604, the power consumption of the portable telephone can be reduced.

Fig. 20B is an on-board audio system (car audio system), containing a main body 2701, a display portion 2702, and operation switches 2703 and 2704. The EL display device of the present invention can be used in the display portion 2702. Furthermore, an on-board audio system is shown in embodiment 17, but a desktop type audio system may also be used. Note that by displaying white characters in a black background in the display portion 2702, the power consumption can be reduced.

The range of applications of the present invention is thus extremely wide, and it is possible to apply the present invention to electronic devices in all fields. Furthermore, the electronic devices of embodiment 17 can be realized by using any constitution of any combination of embodiments 1 to 16.

By using the present invention, it becomes possible to form a pixel in which TFTs, having optimal performance in response to the specifications required by elements, are formed on the same substrate, and the operation performance and reliability of an active matrix type EL display device can be greatly increased.

Furthermore, by using this type of EL display device as a display, it becomes possible to produce applied products (electronic equipment) having good image quality and durability (high reliability).

What is claimed is:

1. An electro-optical device which comprises a pixel comprising:

a first TFT;

a second TFT which comprises a gate that is electrically connected to the first TFT; and

an EL element electrically connected to the second TFT,

wherein the first TFT comprises an active layer in which 2 or greater number of channel forming regions connected in series are formed.

2. An electro-optical device which comprises a pixel comprising:

a first TFT;

a second TFT which comprises a gate that is electrically connected to the first TFT; and

an EL element electrically connected to the second TFT,

wherein the first TFT comprises an active layer in which 2 or greater number of channel forming regions connected in series are formed, and

a channel width of the second TFT is greater than a channel width of the first TFT.

3. An electro-optical device which comprises a pixel comprising:

a first TFT;

a second TFT which comprises a gate that is electrically connected to the first TFT; and

an EL element electrically connected to the second TFT,

wherein at least the first TFT comprises an active layer in which 2 or greater number of channel forming regions connected in series are formed, and

an equation of $W2/L2 \geqq 5 \times W1/L1$ establishes where a channel length of the second TFT is L2, a channel width of the second TFT is W2, a channel length of the first TFT is L1 and a channel width of the first TFT s W1.

4. An electro-optical device according to claim 3 wherein the channel length of the second TFT (L2) is 0.1 to 50 μm, the channel width of the second TFT (W2) is 0.5 to 30 μm, the channel length of the first TFT (L1) is 0.2 to 18 μm and the channel width of the first TFT (W1) is 0.1 to 5 μm.

5. An electro-optical device according to claim 1, wherein the first TFT is a switching TFT and the second TFT is a current control TFT.

6. An electro-optical device according to claim 2, wherein the first TFT is a switching TFT and the second TFT is a current control TFT.

7. An electro-optical device according to claim 3, wherein the first TFT is a switching TFT and the second TFT is a current control TFT.

8. An eletcro-optical device according to claim 1 wherein a LDD region of the first TFT is formed so as not to overlap a gate electrode of the first TFT by interposing a gate insulating film therebetween, and a portion or all of a LDD region of the second TFT is formed so as to overlap a gate electrode of the second TFT.

9. An eletcro-optical device according to claim 2 wherein a LDD region of the first TFT is formed so as not to overlap a gate electrode of the first TFT by interposing a gate insulating film therebetween, and a portion or all of a LDD region of the second TFT is formed so as to overlap a gate electrode of the second

TFT.

10. An eletcro-optical device according to claim 3 wherein a portion or all of a LDD region of the first TFT is formed so as not to overlap a gate electrode of the first TFT by interposing a gate insulating film therebetween, and a LDD region of the second TFT is formed so as to overlap a gate electrode of the second TFT.

11. An electronic device which comprises an electro-optical device of claim 1.

12. An electronic device which comprises an electro-optical device of claim 2.

13. An electronic device which comprises an electro-optical device of claim 3.

14. An electronic device selected from a group consisting of a video camera, a digital camera, a goggle type display, a car navigation system, a personal computer, a mobile computer, a portable telephone, an electronic book, an image playback device using a recording medium, which comprises an electro-optical device according to claim 1.

15. An electronic device selected from a group consisting of a video camera, a digital camera, a goggle type display, a car navigation system, a personal computer, a mobile computer, a portable telephone, an electronic book, an image playback device using a recording medium, which comprises an electro-optical device according to claim 2.

16. An electronic device selected from a group consisting of a video camera, a digital camera, a goggle type display, a car navigation system, a personal

computer, a mobile computer, a portable telephone, an electronic book, an image playback device using a recording medium, which comprises an electro-optical device according to claim 3.

Abstract of the Disclosure

An object of the present invention is to provide an EL display device having a high operation performance and reliability.

The switching TFT 201 formed within a pixel has a multi-gate structure, which is a structure which imposes an importance on reduction of OFF current value. Further, the current control TFT 202 has a channel width wider than that of the switching TFT to make a structure appropriate for flowing electric current. Morever, the LDD region 33 of the current control TFT 202 is formed so as to overlap a portion of the gate electrode 35 to make a structure which imposes importance on prevention of hot carrier injection and reduction of OFF current value.

09825095.060200

Fig. 1

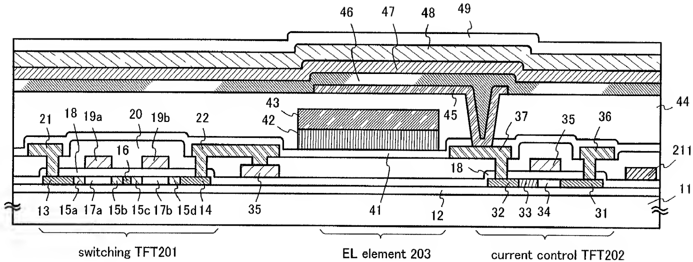


Fig. 2A

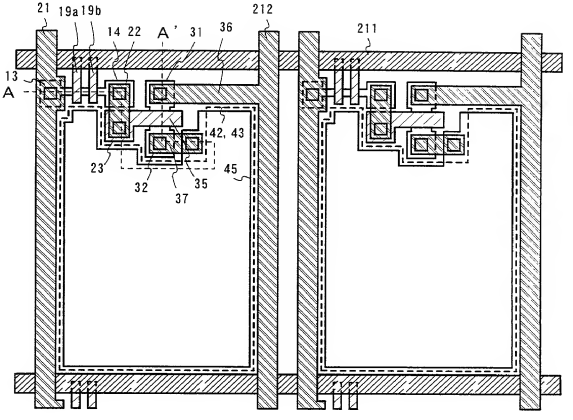

21
19a
19b
14
22
A'
31
36
212
211
13
A
42, 43
23
32
37
35
45

Fig. 2B

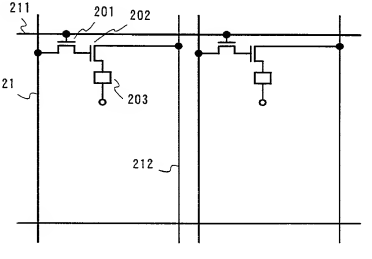

211
201
202
21
203
212

Fig. 3A

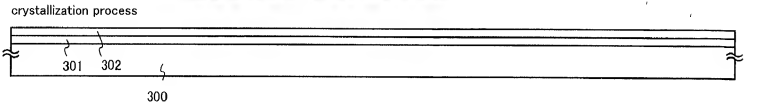


Fig. 3B

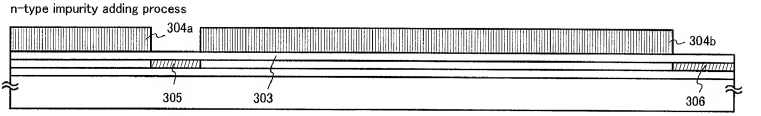


Fig. 3C

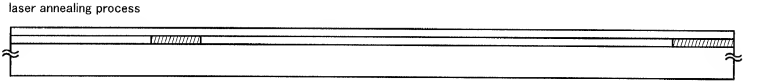


Fig. 3D

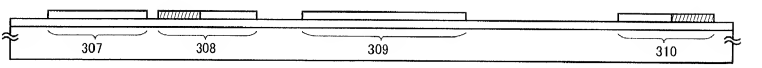
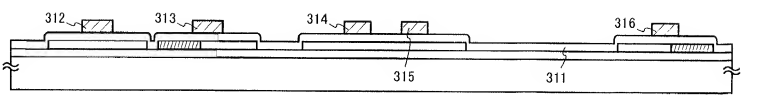


Fig. 3E



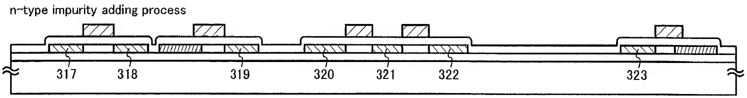


Fig. 4A

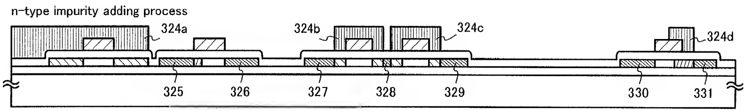


Fig. 4B

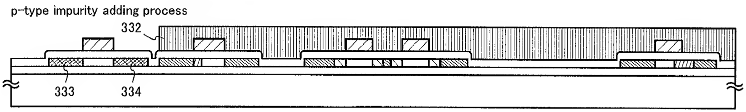


Fig. 4C

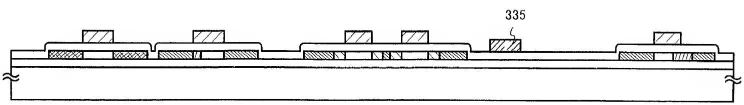


Fig. 4D

Fig. 5A

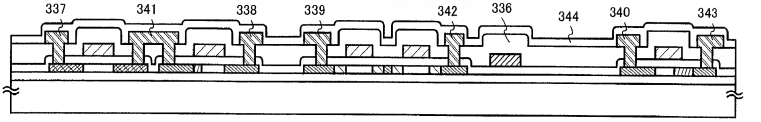


Fig. 5B

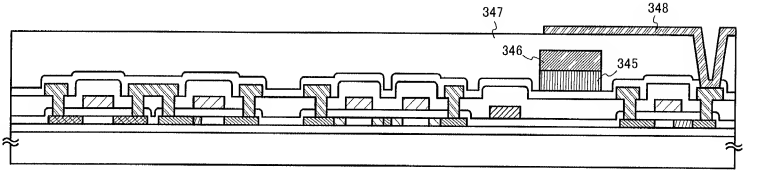


Fig. 5C

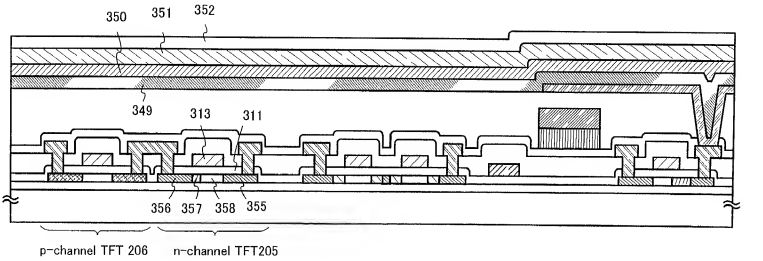


Fig. 6

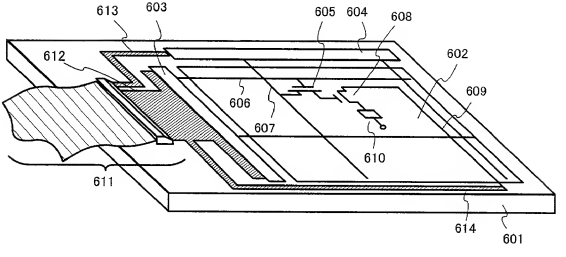


Fig. 7

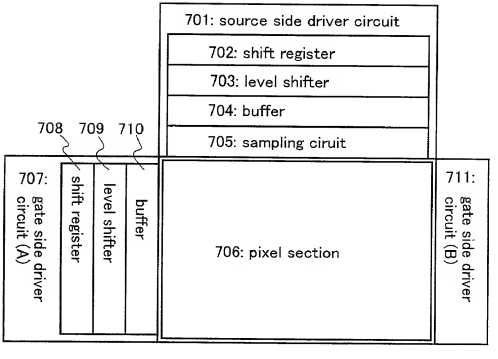

701: source side driver circuit
702: shift register
703: level shifter
704: buffer
705: sampling ciruit
708
709
710
707: gate side driver circuit (A)
shift register
level shifter
buffer
706: pixel section
711: gate side driver circuit (B)

Fig. 8

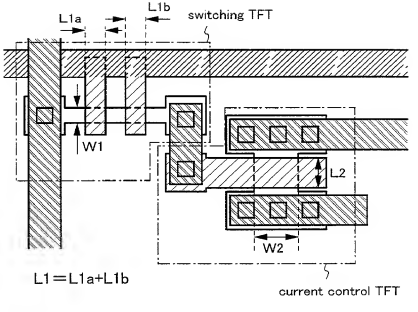


Fig. 9

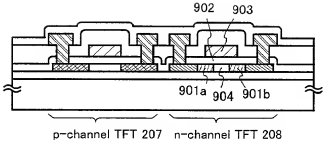


Fig. 10

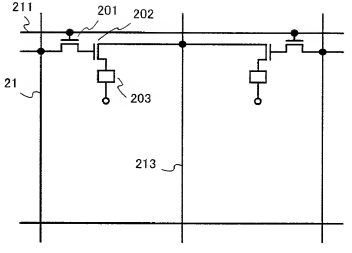


Fig. 11

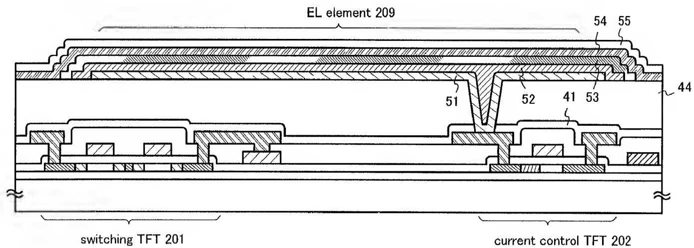

EL element 209
54
55
44
51
52
41
53
switching TFT 201
current control TFT 202

Fig. 12A

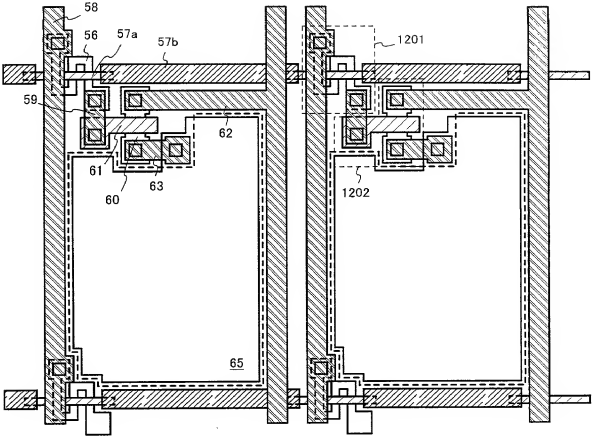


Fig. 12B

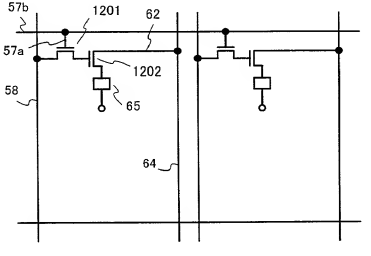


Fig. 13

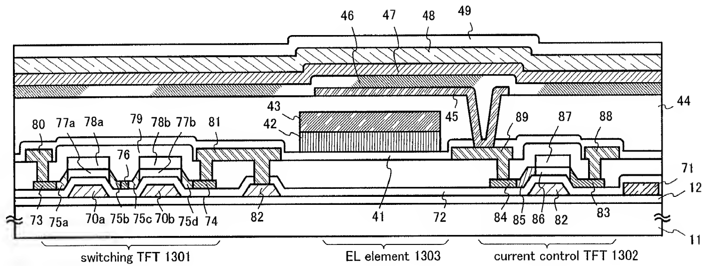


Fig. 14

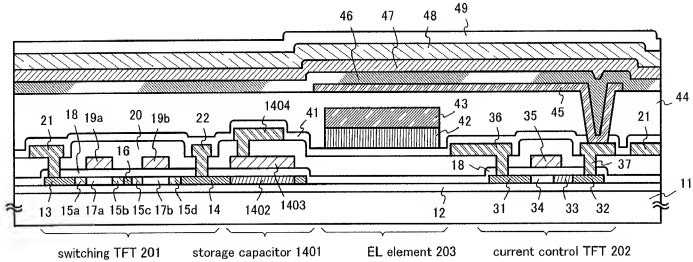


Fig. 15A

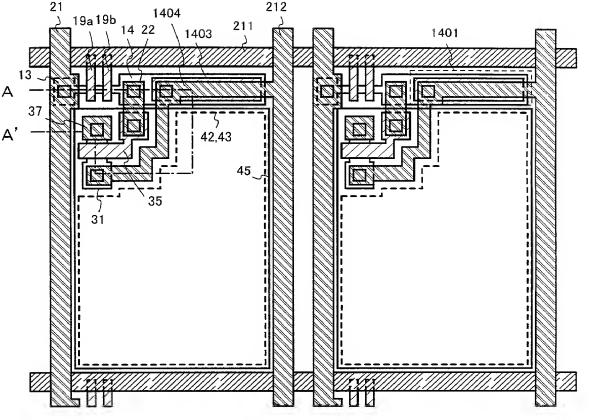


Fig. 15B

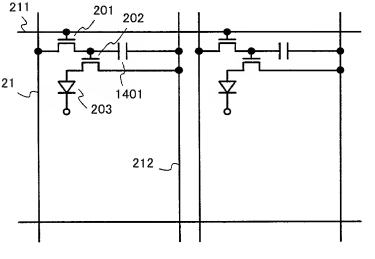


Fig. 16A

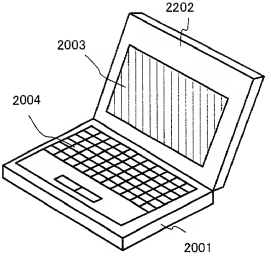


Fig. 16B

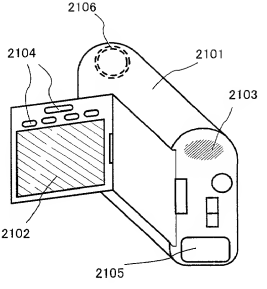


Fig. 16C

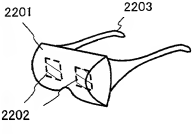


Fig. 16D

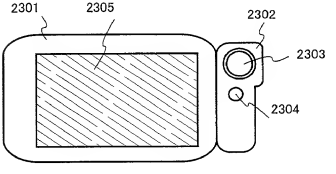


Fig. 16E

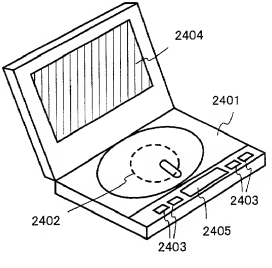


Fig. 16F

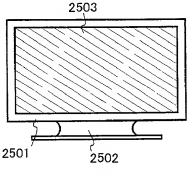


Fig. 17A

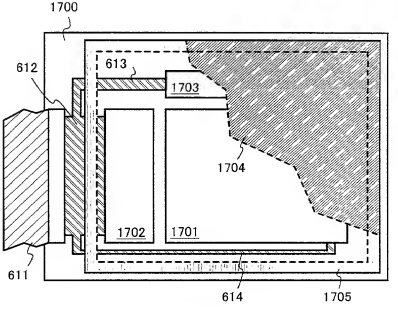


Fig. 17B

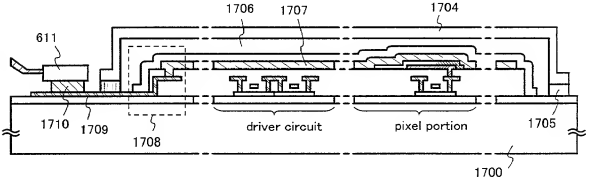


Fig. 18A

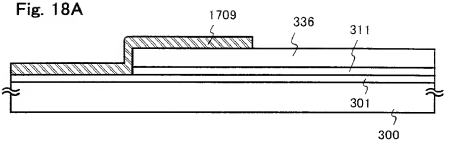


Fig. 18B

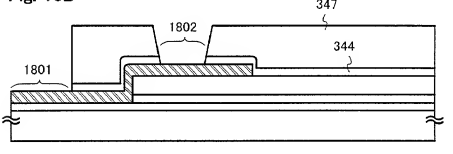


Fig. 18C

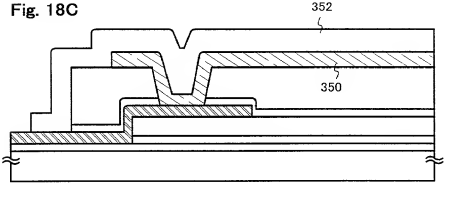


Fig. 19

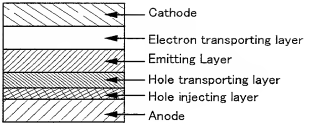

Cathode
Electron transporting layer
Emitting Layer
Hole transporting layer
Hole injecting layer
Anode

Fig. 20A

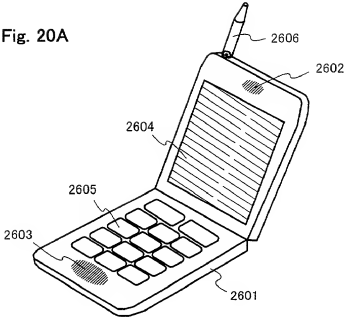


Fig. 20B

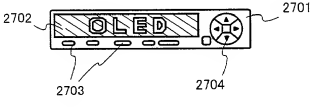


Fig. 21A

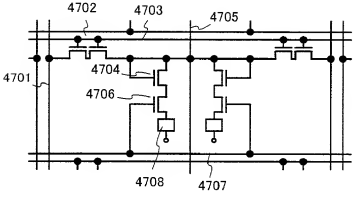


Fig. 21B

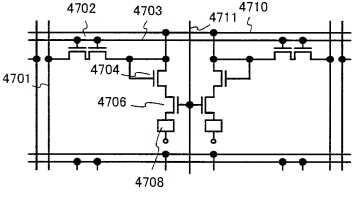


Fig. 22A

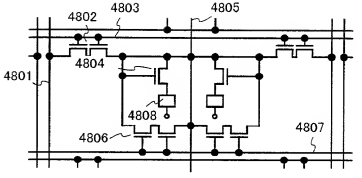


Fig. 22B

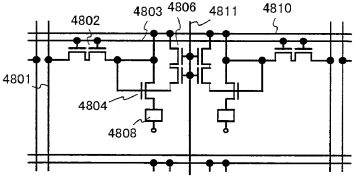
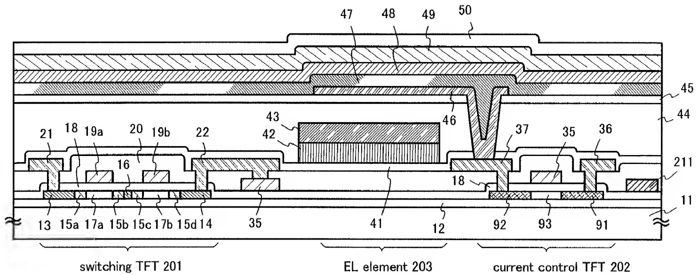


Fig. 23



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17a
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17b
15d
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switching TFT 201
EL element 203
current control TFT 202

Declaration and Power of Attorney For Patent Application
特許出願宣言書及び委任状

Japanese Language Declaration
日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

____

____

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ELECTRO-OPTICAL DEVICE AND ELECTRONIC DEVICE

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を＿＿＿＿＿＿とし、（該当する場合）＿＿＿＿＿に訂正されました。

☐ was filed on ____________ as United States Application Number or PCT International Application Number ____________ and was amended on ______________ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第 37 編第 1 条 56 項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第 35 編 119 条(a)-(d)項又は 365 条(b)項に基き下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約 365(a)項に基く国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

Priority Not Claimed
優先権主張なし

11-158787	Japan	June 4, 1999	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
			☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
			☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	

私は、第35編米国法典119条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第 35 編 120 条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約 365 条(c)に基く権利をここに主張します。また、本出願の各請求範囲の内容が米国法典代 35 編 112 条第 1 項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規制法典第 37 編 1 条 56 項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況: 特許許可済、継続中、放棄済)

(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）

私は、私自身の知識に基いて本宣言書中で私が行う表明が真実であり、かつ私の入手した情報と私の信じるところに基く表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第 18 編第 1001 条に基き、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行えば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状：私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁護士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number).

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Tim L. Brackett (Reg. No. 36, 092)
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Stuart J. Friedman (Reg. No. 24, 312)
Gerald J. Ferguson, Jr. (Reg. No. 23, 016)
Thomas W. Cole (Reg. No. 28, 290)
Jeffrey L. Costellia (Reg. No. 35, 483)
Eric J. Robinson (Reg. No. 38, 285)
Thomas M. Blasey (Reg. No. 33, 475)
Daniel S. Song (Reg. No. 43, 143)

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The undersigned hereby authorizes any U. S. attorney or agent named herein to accept and follow instructions from _____ as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U. S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U. S. attorneys or agents named herein will be so notified by the undersigned.

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